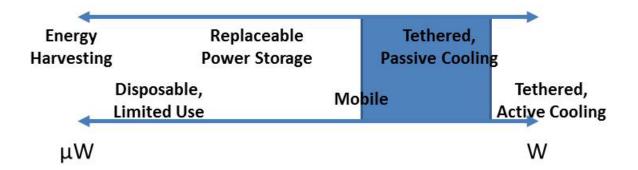# Low Power Optimization Datasheet for

MIPS Technologies

MIPS32 1074K processor core

1. The 1074K targets the shaded portion of the low power spectrum.

2. Operating voltages:

    The operating voltage is dependent on the process the core is implemented into.

3. Typical power at maximum operating frequency

    The operating voltage is dependent on the process the core is implemented into.

4. Clock gating in the 1074K includes fine grained, block level, and top level clock gating in each core (of a multicore system), plus gating based on L1 D-cache way prediction to provides control of dynamic power consumption.

5. Power gating in the 1074K includes a CPU standby mode that is entered via execution of the WAIT instruction. This mode retains the state of the memory.

Multicore power gating enables the system to turn on or off the power to one or more of the cores in the system. It allows the system to scale from a maximum of four (4) cores actively operating down to one (1) core, and back up again. This mode shuts down power completely to the cores to minimize leakage (static) power. Control is provided through the Cluster Power Controller (CPC), which is an IP block included in the MIPS Multicore IP products, that is responsible for voltage and clock gating to the cores in the multicore system.

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6. The semiconductor IP core is a completely static design. The MIPS CPU subsystem can operate at different voltage levels, as defined by the process technology the MIPS CPU is implemented in.

7. The semiconductor IP core is a completely static design. The MIPS CPU subsystem can be frequency and voltage scaled through SoC level control of clock and voltage feeding CPU subsystem.

8. Hardware accelerators include:

- A 64-bit FPU (Floating Point Unit) in the 1074Kf coherent multiprocessing system version
- DSP Application Specific Extensions (ASE) to the base MIPS32 instruction set.
- CorExtend for user-defined instruction set extensions.
- Coherence Manager (CM) unit which maintains L1 cache coherence on data in 1074K (and 1004K) multiprocessor systems.
- IO Coherence Unit (IOCU) – programmable hardware acceleration for maintaining L1 cache coherence in the 1074K cores on I/O traffic from peripherals and DMA engines transferring data directly to/from L2 cache and main memory subsystems.

9. MIPS has multithreading in multiple IP core product lines, including the 34K multithreaded processor, and the 1004K multithreaded coherent multiprocessing system. These products include support for both full Virtual Processing Element (VPE) and lighter weight Thread Context (TC) levels of threading.

However, the 1074K coherent multiprocessing system does not include hardware multithreading. It does include full coherent multiprocessing implementations up to four (4) cores, based on a superscalar, out of order operation, high performance core.

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10. The 1074K coherent processing system (CPS) is a licensable IP product that comes as a complete multiprocessing system. As its name suggests, it includes functionality for closely coupled, cache-coherent multiprocessing. It starts with functionality in the base core pipeline, cache tag arrays, and extension of the interface for coherent snooping and interventions.

The base core connects into a Coherence Manager (CM) unit (included in the 1074K CPS IP), which provides the coherent "fabric" that connects together up to four (4) core implementations of this multiprocessor platform. The CM manages the coherent snooping, interventions and global ordering of operations across the connected cores. The CM supports multiple coherent domains in one multiprocessor system for running multiple operating systems on the same multiprocessor platform. Quad–width internal data paths, cache to cache transfers across cores, and speculative read support to external memory maximize multiprocessing performance.

Three other notable functional elements for multiprocessing support, and included in the 1074K CPS IP, are the IO coherence unit (IOCU), Cluster Power Controller (CPC), and Global Interrupt Controller (GIC). These basically provide the following functionality:

- IOCU – programmable hardware accelerator supporting cache coherence on data traffic generated to/from IO peripherals, with the L1 data caches in the 1074K multiprocessing system.
- CPC – provides clock and voltage/power gating on a per core basis in the 1074K. Register-based control, accessible to software operating systems.
- GIC – Interrupt controller for multicore platform. Supports up to 256 interrupts, with ability to mask and route to a particular core in the system.

A separately licensable L2$ controller IP module, is available from MIPS in use with the 1074K CPS is an L2 cache controller. To maximize bandwidth in use with MIPS multicore IP products, it includes a quad-width (256-wide read and write) OCP-like interface to the coherence manager unit of the 1074K CPS, and provides the option of either 64-bit or 256-bit interface from the L2 cache controller to the external system.

11. The 1074K Coherent Processing System (CPS) datasheet, software user manual, and guide for Programming the 1074K CPS, and application notes are public, non-confidential documents covering the below topics. They can be accessed at http://www.mips.com/products/cores/32-64-bit-cores/mips32-1074k/