Processor Tracker™

MSP43057xx

Texas Instruments' Ultra Low Power FRAM microcontrollers

Information updated: August 8, 2011

Real-time updates for selected processors and development tools

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Welcome to Processor Tracker™

Processor Tracker™ keeps design engineers and marketing groups informed with the initial data and the latest information about selected processors and their supporting ecosystem of development tools.

Processor Tracker™ …

- Is dedicated to selected chips and processor families
- Provides the most up-to-date information available
- Presents important information so that it is understandable at-a-glance
- Saves hours of research across multiple vendor websites
- Warns in real-time of hardware and software changes that can occur without warning or notice
- Covers both embedded and general purpose processors

Please provide feedback about …

- Processors and tools to track
- Data topics to add or remove

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TI's Ultra Low Power FRAM microcontroller
MSP430FR57xx At-A-Glance

This issue of the Processor Tracker and future periodic updates will be dedicated to covering ferroelectric random access memory (FRAM) 16-bit microcontrollers by Texas Instruments Incorporated (TI). According to TI its recently introduced MSP430FR57xx FRAM series ensures data can be written more than 100 times faster and uses as little as 250 times less power than flash- and EEPROM-based microcontrollers. TI's on-chip FRAM additional advantages are data retention in all power modes and support of more than 100 trillion write cycles. The unified memory supported allows developers to easily change memory partitioning between program, data and cache in software, providing inventory management and system cost savings. In the following pages you will find an overview of microcontroller implementations employing FRAM, basic block diagrams and specifications and system development hardware platforms and software tools.

Index of Information Updates

Date	Rev	Document Name / Source URL
July, 2011		FR5739 Data Sheet • Supersedes data sheet dated April 2011 (SLAS639)
4/27/2011	1.0	MSP430FR573x/572x Errata sheet http://focus.ti.com/lit/er/slaz078/slaz078.pdf • Applicability to specific chips • Package Markings • Bugs and workarounds

Table of Contents

Family Description

The Texas Instruments MSP430™ family of ultra-low-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with seven low-power modes is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency.

The MSP430FR572x and MSP430FR573x devices are microcontroller configurations with up to five 16-bit timers, comparator, universal serial communication interfaces (eUSCI) supporting UART, SPI, and I2C, hardware multiplier, DMA, real-time clock module with alarm capabilities, up to 33 I/O pins, and an optional high-performance 10-bit analog-to-digital converter (ADC).

An Overview of MSP430FR57xx FRAM Features

- Embedded Non-Volatile FRAM
  - Supports Universal Memory
  - Ultra-Fast Ultra-Low-Power Write Cycle
  - Error Correction Coding (ECC)
  - Memory Protection Unit
- Low Supply Voltage Range, 2.0 V to 3.6 V
- 16-Bit RISC Architecture, Up to 24-MHz
- Ultra-Low Power Consumption
  - Details on page 7
- Power Management System
  - Fully Integrated LDO
  - Supply Voltage Supervision and Brownout
- Clock System
  - Factory Trimmed DCO with Three Selectable Frequencies (SLAU272)
  - Low-Power/Low-Frequency Internal Clock Source (VLO)
- Five General Purpose 16-bit timers
  - See options in Family Member tables Pages 8-9
- Two Enhanced Serial Interfaces supporting 2 SPI, 1 UART, 1 IrDA, or 1 I2C
  - See options in Family Member tables Pages 8-9
- 10-Bit Analog-to-Digital (A/D) Converter
  - Incorporates Internal Reference & Sample-and-Hold
- On-chip Comparator
- Hardware Multiplier supporting 32-bit operations
- Three channel internal DMA

Industry's first ultra-low-power FRAM microcontroller from TI enables developers to make the world smarter

More data from new places is made possible by the MSP430FR57xx FRAM microcontroller series that allows developers to write up to 100x times faster and save as much as 250x power

DALLAS, May 3, 2011 /PRNewswire/ -- Ushering in a new era of reliable data logging and RF communication capabilities, Texas Instruments Incorporated (TI) (NYSE: TXN) today announced the industry's first ultra-low-power ferroelectric random access memory (FRAM) 16-bit microcontrollers. Further demonstrating TI's embedded processing leadership, the new MSP430FR57xx FRAM series ensures data can be written more than 100 times faster and uses as little as 250 times less power than flash- and EEPROM-based microcontrollers. Additionally, the on-chip FRAM allows data retention in all power modes, supports more than 100 trillion write cycles, and delivers a new dimension of flexibility by allowing developers to partition data and programming memory with changes in software. The FR57xx series eliminates existing power consumption and write endurance barriers, enabling developers to make the world smarter with more cost-efficient data logging, remote sensing and wireless update capabilities in new products that do more and last longer. For more information on TI's new FR57xx microcontrollers with proven FRAM memory, go to www.ti.com/fr57xx-pr-lp.

Key features and benefits of the MSP430FR57xx FRAM microcontrollers

- Reduces the industry's best active power by up to 50 percent when executing code from FRAM, operating at 100uA/MHz in active mode and 3 uA in real-time clock mode
- More than 100 trillion write cycle endurance supports continuous data logging, eliminating need for costly external EEPROM and battery-backed SRAM
- Unified memory allows developers to easily change memory partitioning between program, data and cache in software, providing inventory management and system cost savings
- Guaranteed write and data retention in all power modes ensure code safety to simplify the development process, reduce memory test costs and increase end-product reliability
- Enables reliable remote software upgrades – especially over the air – to provide cheaper, easier software upgrade paths for device manufacturers
- Integrated FRAM densities up to 16kB as well as analog and connectivity peripheral options, including 10-bit ADC, 32-bit hardware multiplier, up to five 16-bit timers and multiple enhanced SPI/I2C/UART buses
- Code compatibility across MSP platform as well as low-cost, easy-to-use tools, comprehensive documentation, user guide and code examples allow developers to get started immediately
- Simplify system development with broad compatible RF tools from TI
- Enables intelligent batteryless RF connectivity solutions
- FR57XX MCUs are built on TI's advanced low power, 130nm embedded FRAM process

Pricing and availability The new MSP430FR57xx microcontrollers start at $1.20 at 10K units, and samples and tools are immediately available. The MSP-EXP430FR5739 Experimenter's Kit is $29 and can be ordered at www.ti.com/fr57xx-pr-ek-es and the MSP-TS430RHA40A Development Kit is $99 and can be ordered at www.ti.com/fr57xx-pr-dk-es.

An Overview of Implementations

The following several pages taken from Texas Instruments' data are showing two of the detailed block diagrams that describe options available with different MCUs.

All of the FRAM MCUs offered employ the same CPU core: the MSP430 CPU: a 16-bit RISC one cycle per register operation 51-instruction architecture that employing high level language can become highly transparent to the application. All operations, other than program-flow instructions, are performed as register to register operations in conjunction with seven addressing modes for source operands and four addressing modes for destination operands.

A three-segment memory protection unit is also common to the different MCU configurations offered -- as is a slave hardware multiplier that can operate on 8- 16- 24- and 32-bit data.

Some of the main optional differences among the FRAM MCUs aside from memory sizes, are in operating frequency that can be either 8MHz or 24MHz (requires FRAM wait states), and the presence or absence of A/D converters and voltage reference.

In its product preview from which we calculate power requirements, Texas Instruments states that with all system clocks active and program execution from FRAM, at 8MHz, a typical power of 2.472mW will be required from a 3.0V power supply.

Similar execution from on-board RAM requires only 1.440 mW due to the higher energy required to read FRAM memory and possibly a level of buffers intended to match FRAM specifications to the on-board buses.

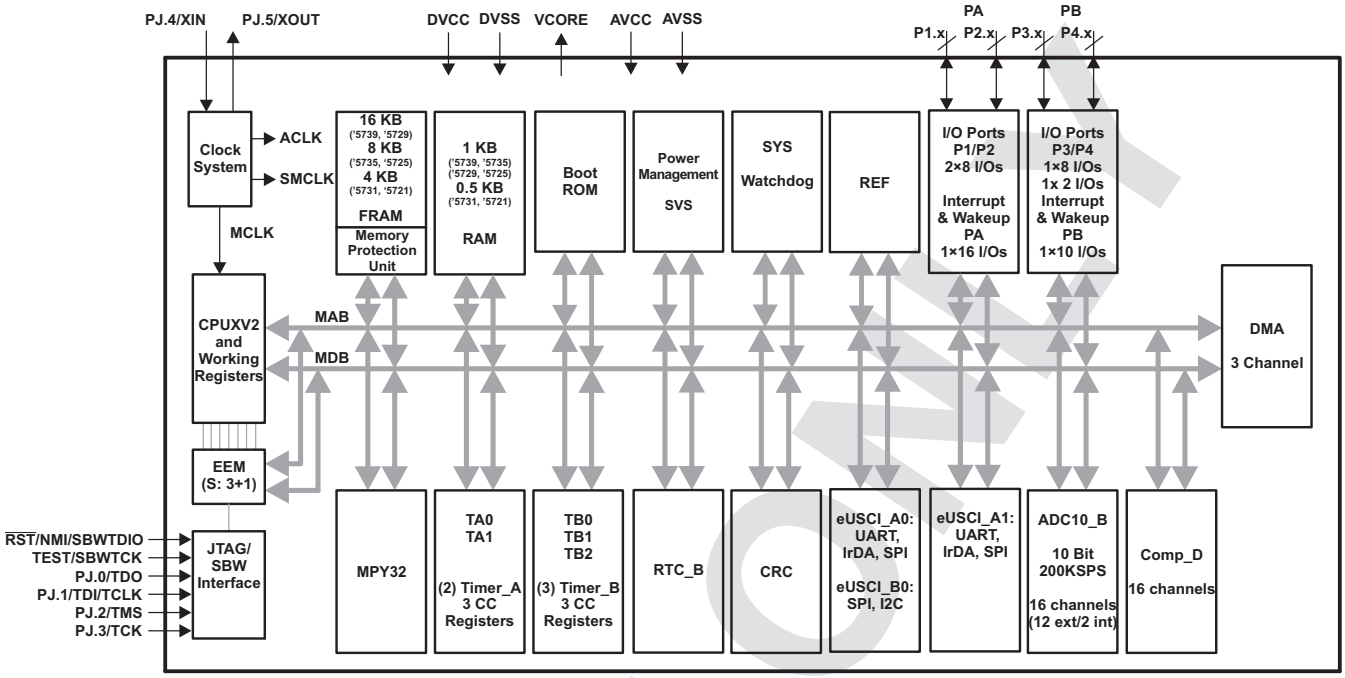
The power requirement drops significantly to a typical 6.3 microAmps (6.4 microAmps with external crystal) for a standby mode that continues to allow quick response via operational real-time clock, watchdog, supply supervisor, and full system state retention.

The recommended operating conditions between -40 degrees C and +85 degrees C are Vcc levels between 2.0V and 3.6V for frequencies between 8MHz and 24MHz.

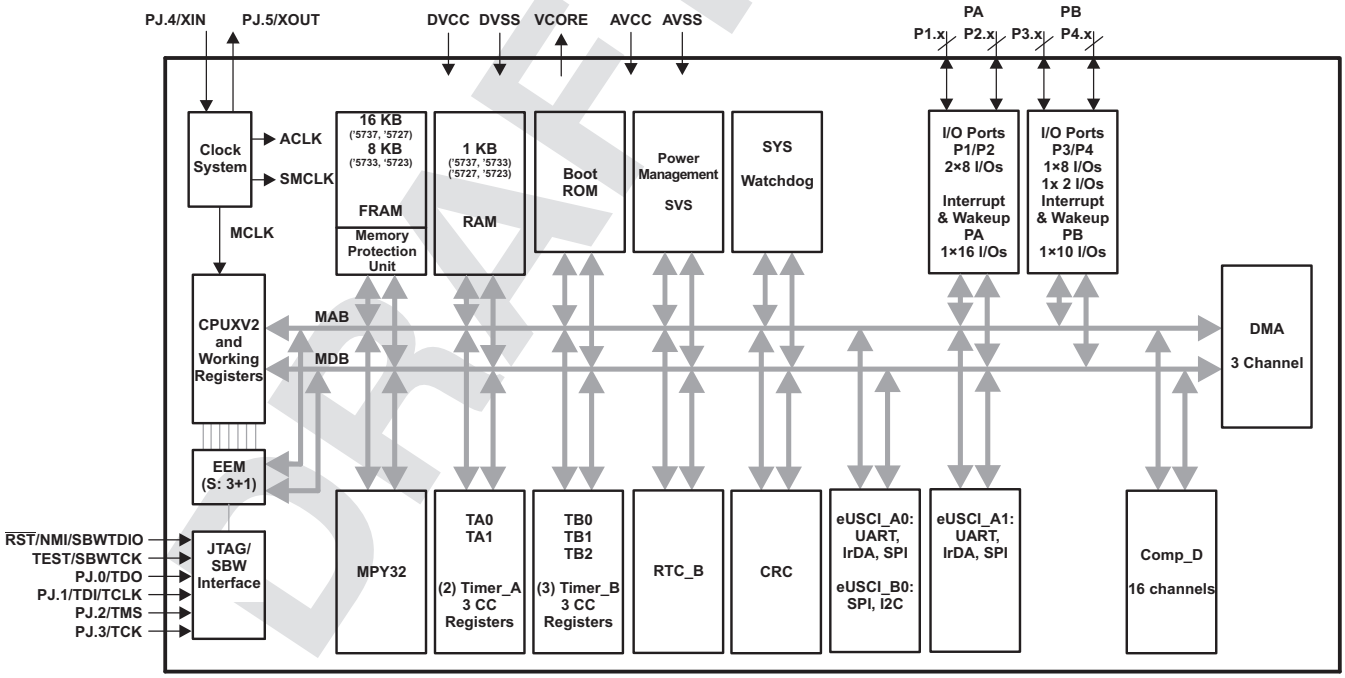
For more detailed specifications please visit
http://focus.ti.com/lit/ds/symlink/msp430fr5739.pdf.

PRODUCT PREVIEW

Functional Block Diagram – MSP430FR5721IRHA, MSP430FR5725IRHA, MSP430FR5729IRHA MSP430FR5731IRHA MSP430FR5735IRHA, MSP430FR5739IRHA



Functional Block Diagram – MSP430FR5723IRHA, MSP430FR5727IRHA MSP430FR5733IRHA, MSP430FR5737IRHA



MIXED SIGNAL MICROCONTROLLER

FEATURES

- Embedded Non-Volatile FRAM
  - Supports Universal Memory
  - Ultra-Fast Ultra-Low-Power Write Cycle
  - Error Correction Coding (ECC)
  - Memory Protection Unit
- Low Supply Voltage Range, 2.0 V to 3.6 V
- 16-Bit RISC Architecture, Up to 24-MHz
- Low Power Consumption
  - Active Mode (AM):
    All System Clocks Active
    103 µA/MHz at 8 MHz, 3.0 V, FRAM Program Execution (Typical)
    60 µA/MHz at 8 MHz, 3.0 V, RAM Program Execution (Typical)
  - Standby Mode (LPM3):
    Real-Time Clock With Crystal , Watchdog, and Supply Supervisor Operational, Full System State Retention:
    6.4 µA at 3.0 V (Typical)
    Low-Power Oscillator (VLO), General-Purpose Counter, Watchdog, and Supply Supervisor Operational, Full System State Retention:
    6.3 µA at 3.0 V (Typical)
  - Off Mode (LPM4):
    Full System State Retention, Supply Supervisor Operational:
    5.9 µA at 3.0 V (Typical)
  - Real-Time Clock Mode (LPM3.5):
    1.5 µA at 3.0 V (Typical)
  - Shutdown Mode (LPM4.5):
    0.32 µA at 3.0 V (Typical)
- Power Management System
  - Fully Integrated LDO
  - Supply Voltage Supervision and Brownout
- Clock System
  - Factory Trimmed DCO With Three Selectable Frequencies
  - Low-Power/Low-Frequency Internal Clock Source (VLO)
  - 32-kHz Watch Crystals and High-Frequency Crystals up to 24 MHz
- 16-Bit Timer TA0, Timer_A With Three Capture/Compare Registers
- 16-Bit Timer TA1, Timer_A With Three Capture/Compare Registers
- 16-Bit Timer TB0, Timer_B With Three Capture/Compare Shadow Registers
- 16-Bit Timer TB1, Timer_B With Three Capture/Compare Shadow Registers
- 16-Bit Timer TB2, Timer_B With Three Capture/Compare Shadow Registers
- Enhanced Universal Serial Communication Interfaces
  - eUSCI_A0 and eUSCI_A1 Each Supporting
    - Enhanced UART supporting Auto-Baudrate Detection
    - IrDA Encoder and Decoder
    - Synchronous SPI
  - eUSCI_B0 Supporting
    - I^2C With Multi-Slave Addressing
    - Synchronous SPI
- 10-Bit Analog-to-Digital (A/D) Converter With Internal Reference, Sample-and-Hold
- On-chip Comparator
- Hardware Multiplier Supporting 32-Bit Operations
- Three Channel Internal DMA
- Real-Time Clock with Calendar and Alarm Functions
- Serial Onboard Programming, No External Programming Voltage Needed
- Family Members and Available Options Are Summarized in Table 1.
- For Complete Module Descriptions, See the *MSP430FR57xx Family User's Guide* (SLAU272)

CAUTION These products use FRAM non-volatile memory technology. FRAM retention is sensitive to extreme temperatures, such as those experienced during reflow or hand soldering. See Absolute Maximum Ratings for more information.

PRODUCT PREVIEW

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

MSP430 is a trademark of Texas Instruments.
I^2C is a trademark of others.

DESCRIPTION

The Texas Instruments MSP430™ family of low-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with seven low-power modes is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency.

The MSP430FR572x and MSP430FR573x devices are microcontroller configurations with up to five 16-bit timers, comparator, universal serial communication interfaces (eUSCI) supporting UART, SPI, and I2C, hardware multiplier, DMA, real-time clock module with alarm capabilities, up to 32 I/O pins, and an optional high-performance 10-bit analog-to-digital converter (ADC). Family members available are summarized in Table 1.

Table 1. Family Members

Device	FRAM (KB)	SRAM (KB)	System Clock (MHz)	ADC10_B	Comp_D	Timer_A(1)	Timer_B(2)	eUSCI		I/O	Package Types
								Channel A: UART/ IrDA/SPI	Channel B: SPI/I²C		
MSP430FR5739	16	1	24	12 ext / 2 int ch.	16 ch.	3, 3	3, 3, 3	2	1	32	RHA
										30	DA
MSP430FR5738	16	1	24	6 ext / 2 int ch.	10 ch.	3, 3	3	1	1	17	RGE
				8 ext / 2 int ch.	12 ch.					21	PW(3)
MSP430FR5737(3)	16	1	24		16 ch.	3, 3	3, 3, 3	2	1	32	RHA(3)
										30	DA(3)
MSP430FR5736(3)	16	1	24		10 ch.	3, 3	3	1	1	17	RGE(3)
					12 ch.					21	PW(3)
MSP430FR5735	8	1	24	12 ext / 2 int ch.	16 ch.	3, 3	3, 3, 3	2	1	32	RHA
										30	DA(3)
MSP430FR5734(3)	8	1	24	6 ext / 2 int ch.	10 ch.	3, 3	3	1	1	17	RGE(3)
				8 ext / 2 int ch.	12 ch.					21	PW(3)
MSP430FR5733(3)	8	1	24		16 ch.	3, 3	3, 3, 3	2	1	32	RHA(3)
										30	DA(3)
MSP430FR5732(3)	8	1	24		10 ch.	3, 3	3	1	1	17	RGE(3)
					12 ch.					21	PW(3)
MSP430FR5731(3)	4	0.5	24	12 ext / 2 int ch.	16 ch.	3, 3	3, 3, 3	2	1	32	RHA(3)
										30	DA(3)
MSP430FR5730	4	0.5	24	6 ext / 2 int ch.	10 ch	3, 3	3	1	1	17	RGE
				8 ext / 2 int ch.	12 ch.					21	PW(3)
MSP430FR5729	16	1	8	12 ext / 2 int ch.	16 ch.	3, 3	3, 3, 3	2	1	32	RHA
										30	DA
MSP430FR5728	16	1	8	6 ext / 2 int ch.	10 ch.	3, 3	3	1	1	17	RGE
				8 ext / 2 int ch.	12 ch.					21	PW(3)
MSP430FR5727(3)	16	1	8		16 ch.	3, 3	3, 3, 3	2	1	32	RHA(3)
										30	DA(3)
MSP430FR5726(3)	16	1	8		10 ch.	3, 3	3	1	1	17	RGE(3)
					12 ch.					21	PW(3)

(1) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_A, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.
(2) Each number in the sequence represents an instantiation of Timer_B with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_B, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.
(3) Product Preview

Table 1. Family Members (continued)

Device	FRAM (KB)	SRAM (KB)	System Clock (MHz)	ADC10_B	Comp_D	Timer_A[1]	Timer_B[2]	eUSCI		I/O	Package Types
								Channel A: UART/ IrDA/SPI	Channel B: SPI/I²C		
MSP430FR5725	8	1	8	12 ext / 2 int ch.	16 ch.	3, 3	3, 3, 3	2	1	32	RHA
										30	DA[3]
MSP430FR5724[3]	8	1	8	6 ext / 2 int ch.	10 ch.	3, 3	3	1	1	17	RGE[3]
				8 ext / 2 int ch.	12 ch.					21	PW[3]
MSP430FR5723[3]	8	1	8		16 ch.	3, 3	3, 3, 3	2	1	32	RHA[3]
										30	DA[3]
MSP430FR5722[3]	8	1	8		10 ch.	3, 3	3	1	1	17	RGE[3]
					12 ch.					21	PW[3]
MSP430FR5721[3]	4	0.5	8	12 ext / 2 int ch.	16 ch.	3, 3	3, 3, 3	2	1	32	RHA[3]
										30	DA[3]
MSP430FR5720	4	0.5	8	6 ext / 2 int ch.	10 ch.	3, 3	3	1	1	17	RGE
				8 ext / 2 int ch.	12 ch.					21	PW[3]

Table 2. Ordering Information[1]

T_A	PACKAGED DEVICES[2]			
	PLASTIC 40-PIN VQFN (RHA)	PLASTIC 24-PIN VQFN (RGE)	PLASTIC 38-PIN TSSOP (DA)	PLASTIC 28-PIN TSSOP (PW)
–40°C to 85°C	MSP430FR5721IRHA[3]	MSP430FR5720IRGE	MSP430FR5721IDA[3]	MSP430FR5720IPW[3]
	MSP430FR5723IRHA[3]	MSP430FR5722IRGE[3]	MSP430FR5723IDA[3]	MSP430FR5722IPW[3]
	MSP430FR5725IRHA	MSP430FR5724IRGE[3]	MSP430FR5725IDA[3]	MSP430FR5724IPW[3]
	MSP430FR5727IRHA[3]	MSP430FR5726IRGE[3]	MSP430FR5727IDA[3]	MSP430FR5726IPW[3]
	MSP430FR5729IRHA	MSP430FR5728IRGE	MSP430FR5729IDA	MSP430FR5728IPW[3]
	MSP430FR5731IRHA[3]	MSP430FR5730IRGE	MSP430FR5731IDA[3]	MSP430FR5730IPW[3]
	MSP430FR5733IRHA[3]	MSP430FR5732IRGE[3]	MSP430FR5733IDA[3]	MSP430FR5732IPW[3]
	MSP430FR5735IRHA	MSP430FR5734IRGE[3]	MSP430FR5735IDA[3]	MSP430FR5734IPW[3]
	MSP430FR5737IRHA[3]	MSP430FR5736IRGE[3]	MSP430FR5737IDA[3]	MSP430FR5736IPW[3]
	MSP430FR5739IRHA	MSP430FR5738IRGE	MSP430FR5739IDA	MSP430FR5738IPW[3]

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/package.
(3) Product Preview

System Development: Hardware Platforms and Software Tools

Texas Instruments is offering two development platforms that can be useful in estimating the capabilities of its FRAM MCUs in addition to writing and debugging final code that does not require linear signal proximity and real-time response from other system components. The two development platforms are the MSP-EXP430FR5739 Experimenter Board and the MSP430FR57xx 40-Pin FET Tool[1] and Target Board Combination, the last one of which can be used with other, non FRAM-employing members of Texas Instruments' MSP430 MCU family.

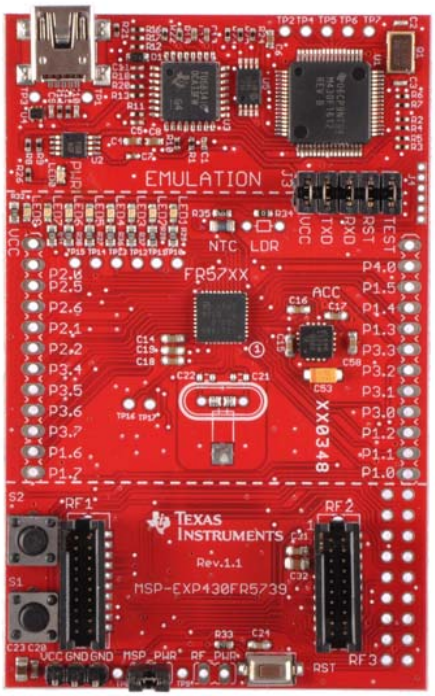
Aside from price, the main differences between the two platforms are the Experimenter Board's availability of pre-programmed demos plus a few peripherals one of which is a very welcome three-axis accelerometer versus the flexibility and debug capability offered by the otherwise bare FET Tool and Target Board Combination that can be used for professional application programming and comparison of FRAM MCUs vs. non-FRAM MCUs from the same family. The experimenter Board can also be employed in coding by overwriting in the FRAM the existing code supplied by Texas Instruments. The existing code can be copied to external memory for reloading to bring back the unit to its initial demo functions. The MSP430FR5739 device on the experimenter board can be powered and debugged via the integrated ezFET, or via a TI Flash Emulation Tool, like the MSP-FET430UIF

Texas Instruments' Code Composer Studio (CCStudio) Integrated Development Environment (IDE) is introduced in the pages following the descriptions of the hardware platforms. More detailed overview information can be found at
http://focus.ti.com/dsp/docs/dspsupportatn.tsp?sectionId=3&tabId=415&familyId=44&toolTypeId=30
A free evaluation copy of CCStudio can be downloaded from
http://focus.ti.com/dsp/docs/dspsupportaut.tsp?sectionId=3&tabId=416&familyId=44&toolTypeId=30
Sample code can be found at
http://focus.ti.com/docs/prod/folders/print/msp430fr5739.html

[1] Flash Emulation Tool can connect a flash-based MSP430 MCU to a PC for real-time, in-system programming and debugging.

System Development Tools*

The MSP-EXP430FR5739 Experimenter Board



Description

The MSP-EXP430FR5739 Experimenter Board is a development platform for the MSP430FR57xx devices. It supports this new generation of MSP430 microcontroller devices with integrated Ferroelectric Random Access Memory (FRAM). The board is compatible with many TI low-power RF wireless evaluation modules such as the CC2520EMK. The Experimenter Board helps designers quickly learn and develop using the new MSP430FR57xx MCUs, which provide the industry's lowest overall power consumption, fast data read /write and unbeatable memory endurance. The MSP-EXP430FR5739 Experimenter Board can help evaluate and drive development for data logging applications, energy harvesting, wireless sensing, automatic metering infrastructure (AMI) and many others. The MSP430FR5739 device on the experimenter board can be powered and debugged via the integrated ezFET.

Features

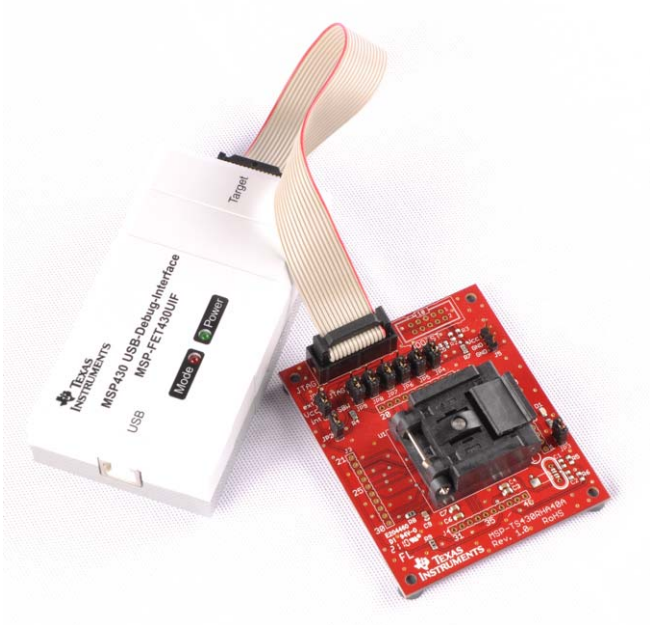
- Integrated MSP430FR5739 :
  - 16KB FRAM / 1KB SRAM
  - 16-Bit RISC Architecture up to 8-MHz
  - 5 General Purpose 16-bit timers
  - 1x USCI (UART/SPI/IrDA/I2C) Blocks, 16Ch 10-Bit ADC12_B, 16Ch Comp_D, 32 I/Os
- 3 axis accelerometer
- NTC Thermistor
- 8 Display LED's
- Footprint for additional through-hole LDR sensor
- 2 User input Switches
- Connections
  - Connection to MSP-EXP430F5438
  - Connection to most Wireless Daughter Cards (CCxxxx RF)
- User Experience
  - Preloaded with out-of-box demo code
  - 4 Modes to test FRAM features:
    - Mode 1 - Max write speed
    - Mode 2 - Flash write speed emulation
    - Mode 3 - Fast sampling with writes using accelerometer
    - Mode 4 - Fast sampling with writes using Thermistor

* Note: For preproduction sampling use the XMS430FR5739iRHA device (Texas Instruments says that the MSP430FR5739iRHA will be available in September-October, 2011)

The MSP430FR57xx 40-Pin FET Tool and Target Board Combination

Description

The MSP-FET430UIF is a powerful flash emulation tool to quickly begin application development on the MSP430 MCU. It includes USB debugging interface used to program and debug the MSP430 in-system through the JTAG interface or the pin saving Spy Bi-Wire (2-wire JTAG) protocol. The flash memory can be erased and programmed in seconds with only a few keystrokes, and since the MSP430 flash is ultra-low power, no external power supply is required.



The debugging tool interfaces the MSP430 to the included integrated software environment and includes code to start your design immediately. The MSP-FET430UIF development tools supports development with all MSP430 flash devices.

The MSP-TS430RHA40A is a standalone 40-pin ZIF socket target board used to program and debug the MSP430 in-system through the JTAG interface or the Spy Bi-Wire (2-wire JTAG) protocol. The development board supports all MSP430FR57xx Flash parts in a 40-pin QFN package (TI package code: RHA).

Features

- USB debugging interface (MSP-FET430UIF) connects a flash-based MSP430 MCU to a PC for real-time, in-system programming and debugging
- Technical specifications:
  - Software configurable supply voltage between 1.8 and 3.6 volts at 100mA
  - Supports JTAG Security Fuse blow to protect code
  - Supports all MSP430 boards with JTAG header
  - Supports both JTAG and Spy-Bi-Wire (2-wire JTAG) debug protocols
- Development board (MSP-TS430RHA40A) with a 40-pin ZIF socket fitting MSP430 derivatives in 40-pin QFN (RHA) packages includes an LED indicator, JTAG adapter, and header pin-outs for prototyping
- Supports all debugging interfaces using a standard 14-pin JTAG header such as the MSP-FET430UIF

What's Included

- Development board with 40-pin QFN (RHA) ZIF socket (MSP-TS430RHA40A)
- JTAG Header cable
- MSP430 USB debugging Interface (MSP-FET430UIF)
- Two XMS430FR5739iRHA (Texas Instruments says this will be updated to the MSP430FR5739iRHA in September-October, 2011) FRAM memory silicon devices

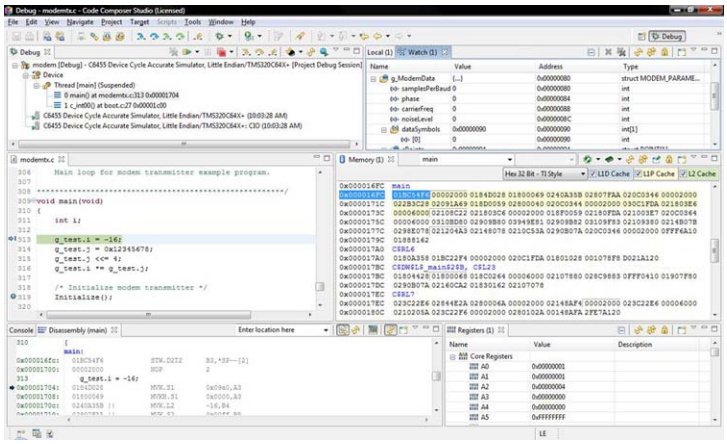
Software Development Tools

Code Composer Studio (CCStudio) Integrated Development Environment (IDE) v4.x

Description

Code Composer Studio v4 (CCStudio v4) is the integrated development environment (IDE) for TI's DSPs, microcontrollers and application processors.

Features



Code Composer Studio IDE includes a suite of tools used to develop and debug embedded applications. It includes compilers for each of TI's device families, source code editor, project build environment, debugger, profiler, simulators and many other features. The CCStudio IDE provides a single user interface taking you through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before and add functionality to their application thanks to sophisticated productivity tools.

As of version 4 CCStudio IDE is based on the Eclipse open source software framework. The Eclipse software framework is used for many different applications, but it was originally developed as an open framework for creating development tools. We have chosen to base CCStudio IDE on Eclipse as it offers an excellent software framework for building software development environments and is becoming a standard framework used by many embedded software vendors. CCStudio IDE combines the advantages of the Eclipse software framework with advanced embedded debug capabilities from Texas Instruments resulting in a compelling feature-rich development environment for embedded developers.

Additional Information:

- Wiki: Support for CCStudio IDE v4
- Overview: CCStudio IDE
- Getting Started with CCStudio IDE
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    - Platinum supports all TI embedded processors.
    - Microcontroller supports only TMS320C2800, MSP430(TM), Stellaris(R) and Cortex(TM)-R4.
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White Paper
SLAA502–June 2011

Low-Power FRAM Microcontrollers and Their Applications

Volker Rzehak *Texas Instruments Deutschland*

Texas Instruments recently announced a new microcontroller family that implements FRAM as non-volatile memory instead of Flash, today's most common programmable, non-volatile memory technology. The paper explains the FRAM technology and how embedded applications can benefit from it.

The physics behind the FRAM technology are briefly covered. The differences and benefits of FRAM versus other non-volatile memory technologies like Flash are shown like the low current consumption, the fast write, and the high write endurance. The concept of "universal memory" is also introduced.

This paper illustrates how embedded applications can benefit from the features the FRAM technology offers such as ultra-low power data loggers and batteryless energy harvesting applications.

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1 What is FRAM?

FRAM stands for Ferroelectric Random Access Memory. (Note there are other acronyms for FRAM used by other companies such as F-RAM or FeRAM.)

As the "RAM" part of the name already suggests, FRAM behaves similarly to DRAM. It allows random access to each individual bit for both read and write. Unlike EEPROM or Flash memory technology, FRAM does not require a special sequence to write data nor does it require a higher programming voltage. But FRAM is non-volatile; that is, it does not "lose" its content when power is removed.

So why is FRAM non-volatile? This is because of the special dielectric material used in the storage capacitor: a ceramic that allows making use of the so-called ferroelectric effect.

The term "ferroelectric" does not mean that the memory contains iron (the chemical element Fe) nor does it imply that the memory can be influenced by magnetic fields. In fact it is immune to magnetic fields.

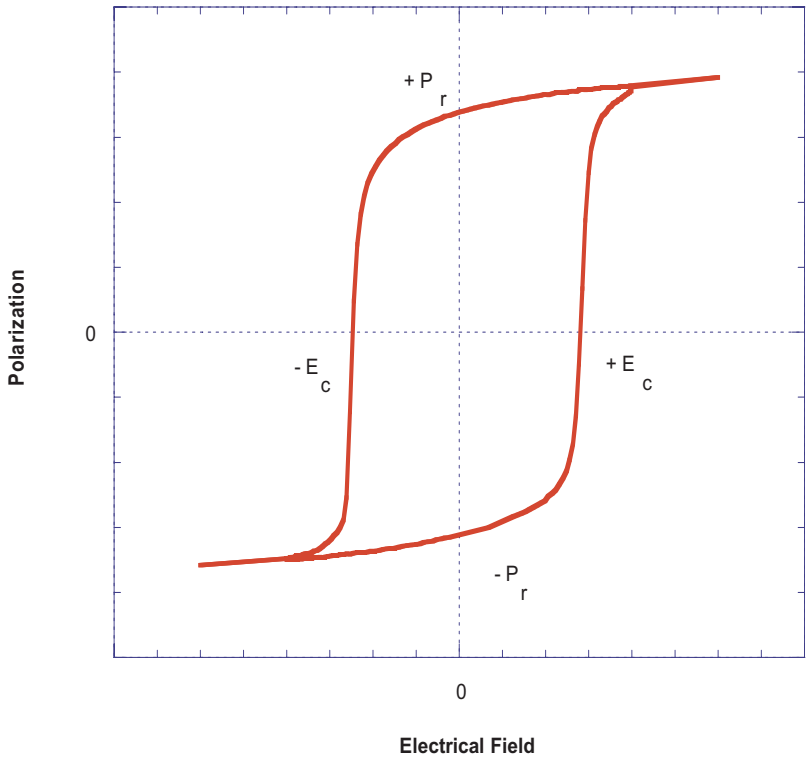

Figure 1. Polarization Hysteresis Loop

The term results from the hysteresis loop (shown in Figure 1) being similar to the magnetic hysteresis loop of iron (Fe). In contrast to the magnetic hysteresis loop, the one in FRAM results from the electrical dipole formed by zirconium (Zr) and oxygen (O) atoms in the ceramic lead-zirkonate-titanate crystal (PZT) used to implement FRAM as shown in Figure 2.

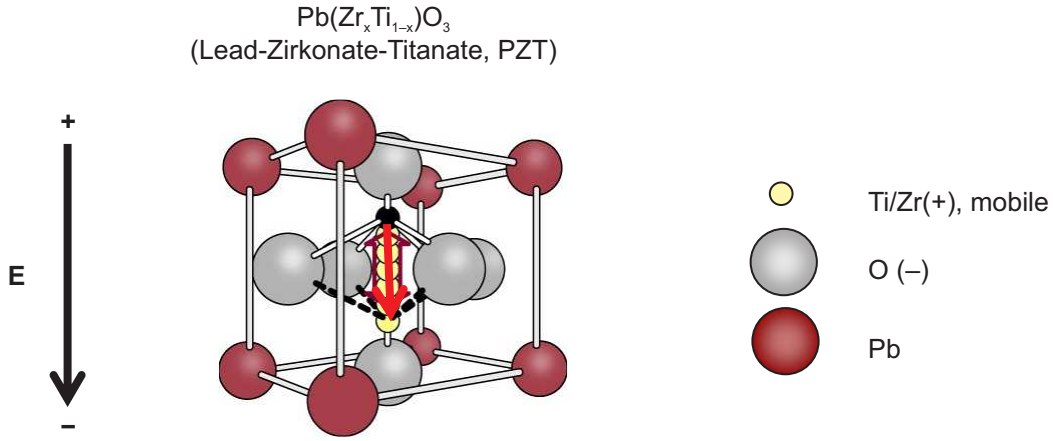

Figure 2. Lead-Zirkonate-Titanate Structure

Applying an electrical field (E) can polarize the material by "moving" the Zi atom in the structure. But to move the Zi atom from one side (here from the upper) to the other side (here the lower) of the O atoms, it must cross the barrier from by the O atoms. So, with increasing field strength, the Zi atom moves gradually closer to the O atoms before – at a certain field strength – it "suddenly" flips to the other side. If a field is then applied with opposite direction, again the Zi atom would just gradually change its position before flipping to the other side. This will happen at the same field strength as before, but with an opposite sign. This behavior results in the electrical field versus polarization hysteresis loop shown in Figure 1.

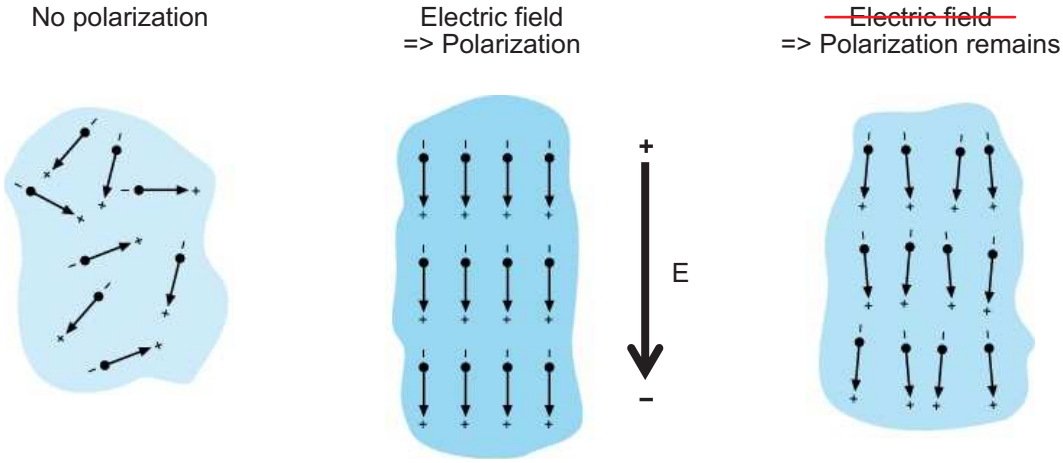

Figure 3. Polarization

After manufacturing, the dipoles formed by the zirconium and oxide atoms are randomly polarized resulting in a net polarization of zero (no polarization). Applying an electric field aligns the dipoles and results in a polarization in the direction defined by the electric field. Because the position of the zirconium atoms within the crystal structure is stable, the polarization remains even after removing the electric field.

2 Why FRAM? – An Application Example

In the following example, the benefits of an FRAM-based microcontroller are illustrated using a data logger as application example. A data logger is typically a sensor node that collects various physical or environmental conditions like temperature, humidity, vibration, pressure, motion, or pollutants (see Figure 4).

Figure 4. Data Logger

2.1 FRAM: A Universal Memory

In a data logger application, the program code size required to measure and collect the data can be comparably small with respect to the amount of memory to store the data. Assuming the use of external memory is not an option and, thus, the data should be stored in the RAM of a "traditional" flash-based microcontroller, one would have to purchase a device that has excessive program memory compared to what the application needs. With an FRAM-based microcontroller, the available memory can be partitioned to the needs of the application and, thus, a much larger portion can be made available for data to meet the application requirements.

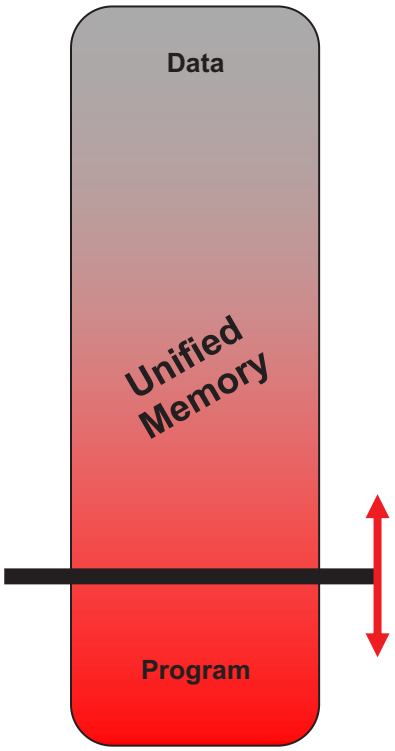

Figure 5. Unified Memory

The concept behind this is called "unified memory". Universal memory allows flexible partitioning of the memory for code and data: the same type of memory can be used for both data and program storage that are "traditionally" kept in separate memories: RAM for data and flash or ROM for program storage.

To support the "unified memory" concept, a Memory Protection Unit (MPU) is implemented in the FRAM-based MSP430 devices from Texas Instruments. The MPU allows for example to "protect" parts of the memory that are used for program storage from being overwritten accidentally.

2.2 Write Endurance

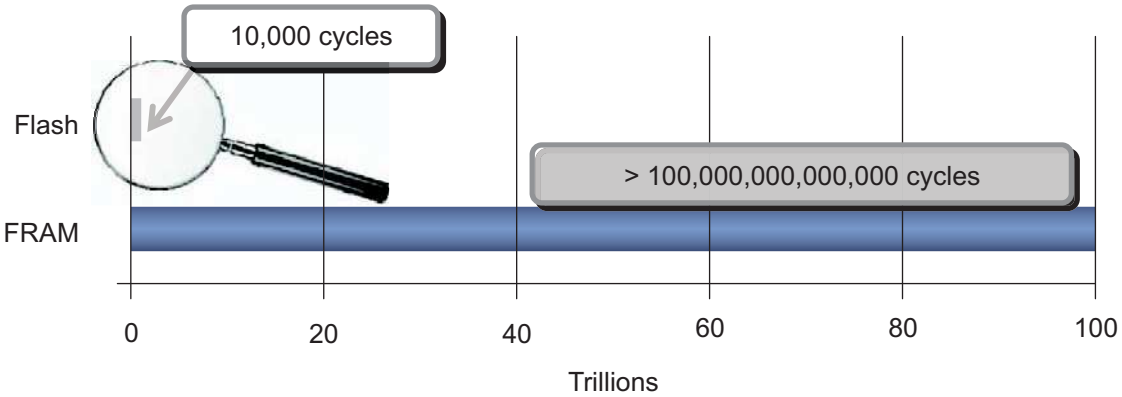

Figure 6. Write Endurance

The FRAM technology provides write endurance that is superior to other non-volatile memory technologies as illustrated in Figure 6. For the data logger application, that translates into a much longer lifetime with less complexity: assuming the data logger has to store one set of data each second and it always uses the same addresses, this would translate into a lifetime of a data logger using Flash memory of less than three hours (assuming a Flash with 104 cycles divided by 1 cycle per second). The same data logger

using FRAM would achieve a theoretical life time of more than 3 million years making use of the more than 10^{14} write cycles FRAM offers. To increase the life time of the Flash-based data logger, complex wear leveling algorithms together with additional Flash memory space would be required. The wear leveling algorithms would try to make use of multiple Flash cells and use them more or less equally. For FRAM, wear leveling is not required, which significantly reduces the complexity and also the amount of memory required.

2.3 Fast Write

An additional benefit of the FRAM technology is its fast write capability.

To write Flash, tens of microseconds to several milliseconds are required to program one data word (for example, the MSP430F5438A specifies between 37 µs and 85 µs to program one word, depending on programming mode and process conditions; for other microcontrollers, programming times in the range of 3 to 5 milliseconds are sometimes specified). This does not include a pre-erasure of the segment to be re-programmed. The pre-erasure will add several milliseconds. In addition, no program execution is usually possible while programming.

In contrast, FRAM requires only ~100 ns to program one data word. Additionally, no pre-erase is required and, because of the fast write, there is virtually no interruption of the program execution.

3 Another Application Example: Light Switch

The following application is a light switch that switches the lights via an RF link and harvests the energy from being switched. This means that the microcontroller and transceiver are not powered most of the time. Because of that, all data that needs to be retained must be stored in a non-volatile memory. The data that must be retained could be, for example, RF network parameters. In an intelligent light switch with dimming, additional status information could be stored.

In a flash-based microcontroller, the programming of a word would require a couple hundred nanocoulomb (nC) of charge (for example: ~100 µs × 2 mA = 200 nC), whereas in a FRAM-based microcontroller, the required charge to program the same amount of bits is on the order of two to three magnitudes (more than 100 times) smaller (for example: ~100 ns × 4 mA = 400 pC). Thus, with the same charge harvested from being switched, more than 100 times of data can be permanently stored with a FRAM-based microcontroller compared to a Flash-based microcontroller. Alternatively, the energy harvesting circuitry can be dimensioned to provide and store less energy.

Of course, this example is applicable to all energy harvesting applications that can be unpowered for a certain time but still need to retain variable data.

Note: the charge required to program can vary from device to device and from manufacturer to manufacturer. The numbers shown here are only examples used to show the magnitude of difference.

4 Other Applications

FRAM-based microcontrollers can be used for any application where microcontrollers with a different non-volatile memory technology like Flash or EEPROM are currently used. However, certain application can specifically benefit from the FRAM technology, and other applications might only be possible with FRAM as memory.

A few additional applications or application scenarios are listed that specifically can benefit from the features an FRAM-based microcontroller offers:

- Data logger applications
- Energy harvesting application
- Applications with "Over the Air Updates"
- Replacement of external EEPROM

5 MSP430FR57xx Family

Beyond integrating FRAM as their main memory technology, the MSP430FR57xx family devices have other unique features suck as an extremely low active mode current consumption of ~100 µA/MHz. They also offers a rich mixture of peripherals including communication ports, timers, and a 10-bit ADC with integrated reference (see the block diagram in Figure 7).

The MSP430FR57xx family offers 20 different devices with FRAM memories up to 16kB. The devices are offered in four packages ranging from a tiny 24-pin QFN to a 40-pin QFN, as well 28-pin and 38-pin TSSOP packages.

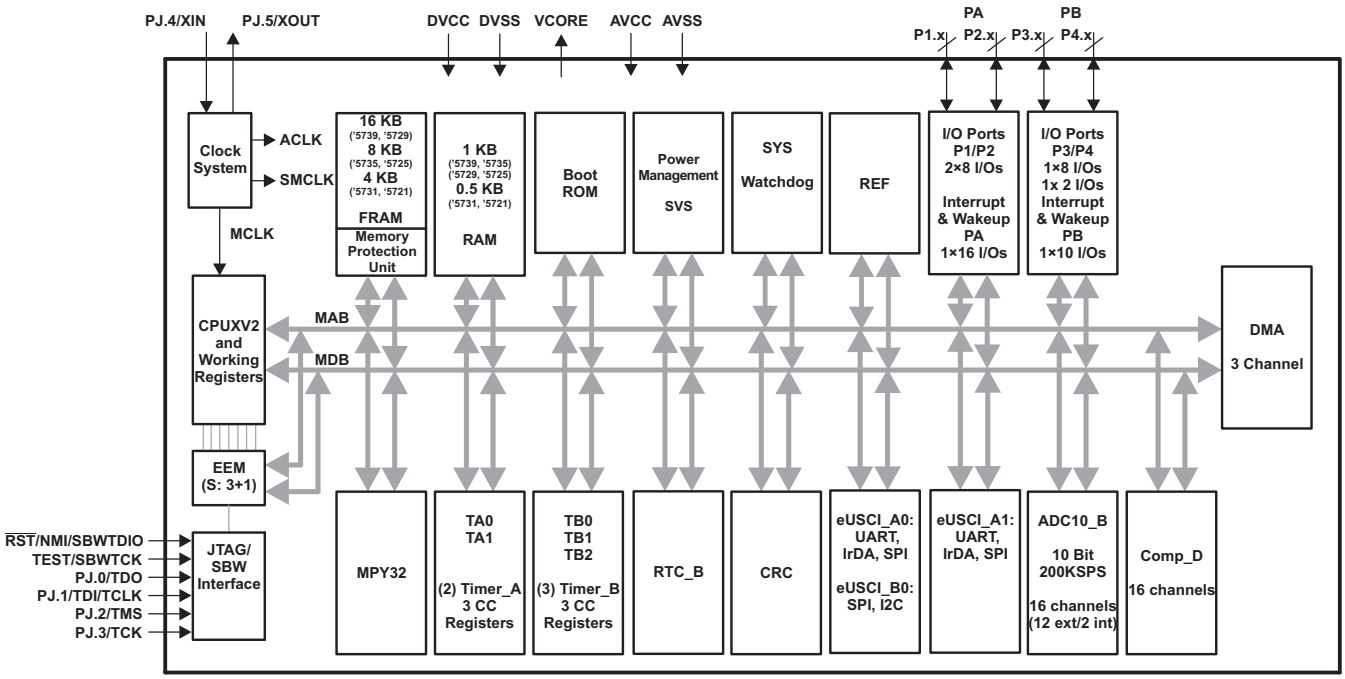

Figure 7. MSP430FR57xx Family Block Diagram

6 Conclusion

A microcontroller with integrated FRAM provides a non-volatile memory that can be used for both data and code storage (unified memory), is low-power, can be written quickly, and offers practically unlimited write endurance.

The FRAM-based microcontrollers can be used in nearly every MCU-based application, and their unique features may enable new applications we currently might not even think of.

7 References

TI's FRAM page: http://www.ti.com/fram

General FRAM information at http://en.wikipedia.org/wiki/Ferroelectric_RAM

MSP430FR57xx data sheet (SLAS639)

MSP430F5438A data sheet (SLAS655)

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Application Report
SLAA498–June 2011

Maximizing FRAM Write Speed on the MSP430FR573x

Priya Thanigai *MSP430 Applications*

ABSTRACT

Non-volatile, low-power FerroElectric RAM (FRAM) is capable of extremely high speed write accesses. This application report discusses how to maximize FRAM write speeds specifically in the MSP430FR573x family using simple techniques. The document uses examples from bench tests performed on the MSP430FR5739 device and discusses tradeoffs such as CPU clock frequency and block size and how they impact the FRAM write speed.

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1 Introduction to FRAM

FRAM is a non-volatile memory technology that behaves similar to the widely used volatile static RAM (SRAM). It has all the advantages that can be attributed to SRAM, such as being bit-addressable with no requirements for pre-erase, while being non-volatile. The MSP430FR5739 is the world's first embedded FRAM solution with a 16-bit ultra low power MCU.

There are a few significant differences between the MSP430FR5739 and other MSP430™ Flash offerings, some of which are outlined in *Migrating From the MSP430F2xx Family to the MSP430FR57xx Family* (SLAA499).

The purpose of this application report is to provide a brief introduction to FRAM while discussing typical application use cases and how they can be implemented to improve FRAM write speed. There are a couple of main differences between FRAM and SRAM:

- FRAM is non-volatile, i.e., it retains contents on loss of power.
- The embedded FRAM on MSP430 devices can be accessed (read/write) at up to a maximum speed of 8 MHz.

In comparison to MSP430 Flash[1], FRAM:

- Is very easy to use
- Requires no setup or preparation such as unlocking of control registers
- Memory is not segmented and each bit is individually erasable, writable, and addressable
- Does not require an erase before a write
- Allows low-power write accesses (does not require a charge pump)
- Can be written to across the full voltage range (2.0 V-3.6 V)
- Can be written to at speeds close to 8 MBps (maximum Flash write speed including the erase time is ~14k Bps)
- Uses wait-states when accessed at speeds > 8 MHz

A comparison between Flash, FRAM and static RAM is given in Table 1.

[1] All MSP430 Flash data references the *MSP430F22x2, MSP430F22x4 Mixed Signal Microcontroller Data Sheet* (SLAS504).

Table 1. Comparison Between Embedded Memory Technologies

	FRAM	SRAM	Flash
Write speed per word	125 ns	< 125 ns	85 µs
Erase time	No pre-erase required	No pre-erase required	23 ms for 512 bytes
Bit-wise programmable	Yes	Yes	No
Write Endurance	10^14 write/erase cycles	N/A	10^5 write/erase cycles
Non-volatile	Yes	No	Yes
Internal write voltage	1.5 V	1.6 V	12 V-14 V (charge pump required)

2 Writing to FRAM

2.1 The FRAM Write Cycle

All FRAM accesses are limited to 125 ns per access or 8 MHz access frequency. However, the MSP430FR573x family is capable of system speeds (MCLK) up to 24 MHz. Therefore, the FRAM controller automatically inserts wait states to prevent the FRAM from being accessed at speeds higher than 8 MHz. These wait states can also be controlled manually, i.e., programmed in firmware, if the application requires very precise timing for FRAM read/writes. For more details on manual and automatic wait states, see the *MSP430FR5xx Family User's Guide* (SLAU272) [1].

2.2 Theoretical Calculation on the Maximum FRAM Write Speed

The MSP430FR5739 data sheet specifies FRAM word or byte write time t_{WRITE} as 125 ns [2]. This leads to a maximum write time of 8 Mega-words per second or 16 Megabytes per second (MBps). However, this maximum speed is theoretical because it does not account for the time taken for data handling overhead. Small blocks of data require frequent processing for pointer updation and data retrieval when compared to larger blocks. Therefore, one method to increase the speed of FRAM write is to minimize CPU intervention for data handling and use DMA to optimize data transfers.

A second method to optimize the write speed is by increasing the CPU speed beyond 8 MHz, allowing data handling operations that are cached in SRAM to be executed at speeds faster than 8 MHz. These two methods are discussed in greater detail in the following sections.

2.3 Increasing FRAM Write Speed Using DMA

Since FRAM writes are very high speed, the biggest bottleneck lies in the data handling and processing overhead. This may be due to a communication protocol that is limited to a specific speed or due to application overhead caused by data movement and pointer updates. Figure 1 presents an example use case where 2 to 512 bytes are written to FRAM using a simple code example that performs a move and an increment operation at a CPU clock frequency (MCLK) = 8 MHz. This example use case is then compared to writing the same number of bytes but using DMA instead. It can be seen that for smaller block sizes using DMA does not provide any noticeable advantage, but as the block size increases, using DMA minimizes CPU intervention per block, thereby, reducing the overall write time and dramatically increasing FRAM write speed. Figure 1 illustrates, for a block size of 512 bytes, using DMA yields FRAM write speeds that are 4x that when DMA is not used.

Therefore, DMA is the preferred approach to efficiently benchmark the maximum achievable speed when writing to FRAM.

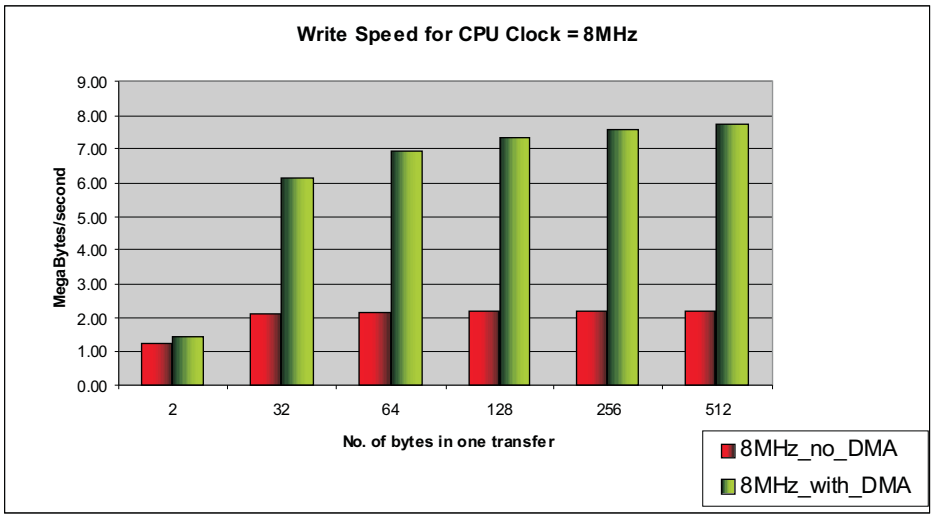

Figure 1. Comparing Write Speeds With and Without DMA Usage

Each DMA transfer takes 2 MCLK cycles. When writing to memory using DMA, a block-wise approach is preferred because the initial overhead for setting up the block is spread over the size of the block. An example code that uses block-wise DMA to write to FRAM is shown. Since FRAM writes are similar to RAM writes there is no special memory handling required.

The code used to benchmark the time taken to write an FRAM block does the following:

- Initializes DMA registers and configures block size
- Toggles general-purpose input/output (GPIO) at the start of a DMA transfer
- Sets the DMA trigger to transfer a block
- Toggles GPIO to indicate the end of DMA transfer

Since the CPU is held while the DMA block transfer is in progress and not released until it is complete, it is not required to check the DMA interrupt flag at the end of a transfer. The GPIO output pin is used to measure the time per DMA block write. The code is written in assembler to avoid any potential overhead or other possible side effects caused by C compilers.

```
SetupData
            mov.w   #0x1D00,R4              ; Data is stored in SRAM @ 0x1D00
            mov.w   #0x1234,0(R4)
SetupPort                                   ; output toggle on P3.6
            bis.b   #BIT6,&P3DIR

SetupDMA
            movx.a  #0x1D00,&DMA0SA         ; Start block address- some RAM location
            movx.a  #0xD000,&DMA0DA         ; Destination block address - FRAM
scratchpad
            mov.w   #1,&DMA0SZ              ; Block size in words 1 to 4096
                                            ; DMA in repeated block, dst increment, word mode
            mov.w   #DMADT_5+DMASRCINCR_0+DMADSTINCR_3,&DMA0CTL
            bic.w   #DMADSTBYTE+DMASRCBYTE,&DMA0CTL
            bis.w   #DMAEN, &DMA0CTL        ; Enable DMA0
Mainloop
            bis.b   #BIT6, &P3OUT           ; Set P3.6 at the start of transfer
            bis.w   #DMAREQ,&DMA0CTL        ; Clear P3.6 at the end of transfer
            bic.b   #BIT6,&P3OUT            ; Trigger block transfer
            jmp     Mainloop
```

The plot of measured FRAM write speed for various DMA block sizes is shown in Figure 2. These measurements were taken with CPU clock frequency = 8 MHz.

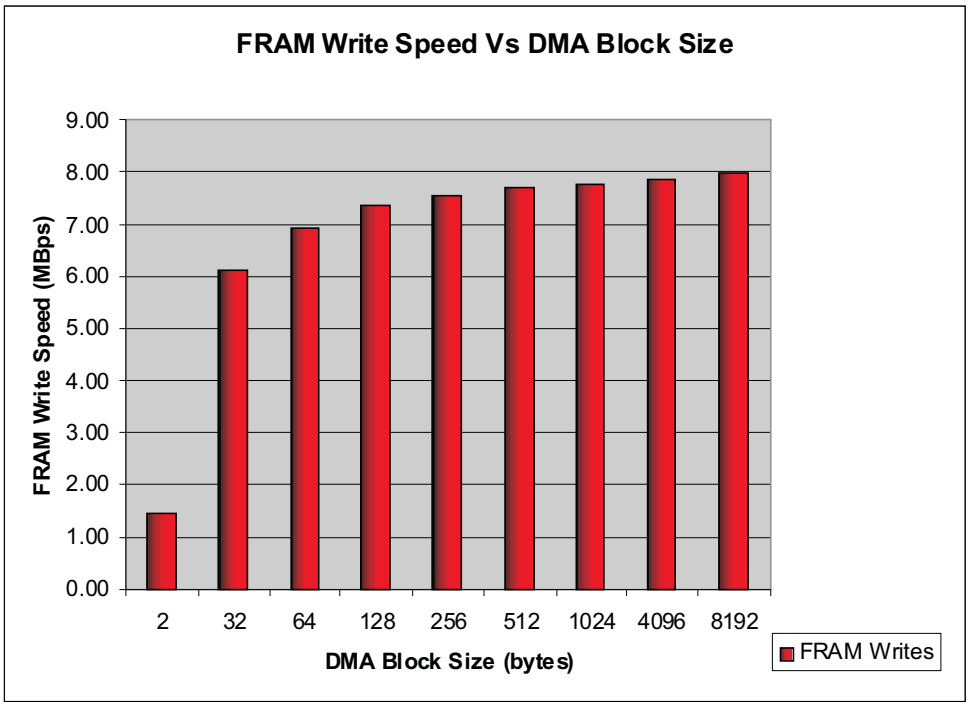

Figure 2. FRAM Write Speed for Various DMA Block Sizes (CPU Clock Frequency = 8 MHz)

Figure 2 shows that for a large block size of 8192 bytes, the write speed of FRAM is close to 8 MBps. This is half the theoretical maximum FRAM write speed according to Section 2.2. The reason for this is that for every FRAM word write – two CPU cycles are spent in the actual data transfer. The smaller the block size, the more time is spent in toggling the GPIO output and re-triggering the DMA when compared to the actual FRAM access. While a large transfer of 8KB is most likely not suitable in all applications, it can be seen that even for a moderate block size of 512 bytes (similar to Flash), the FRAM write speed is ~7.7 MBps and is about 500 times faster than a corresponding 512-byte block Flash write.

Table 2 shows the actual write times and corresponding write speeds for various DMA block sizes.

Table 2. FRAM Write Speed for Various DMA Block Sizes (CPU Clock Frequency = 8 MHz)

	MCLK = 8 MHz	MCLK = 8 MHz
DMA Size (bytes)	Write Time µs	Write Speed MBps
2	1.35	1.45
32	5.1	6.13
64	9.02	6.93
128	17.04	7.34
256	33.14	7.54
512	64.74	7.72
1024	128.3	7.79
4096	509.2	7.86
8192	1002	7.98

2.4 Increasing FRAM Write Speed by Maximizing CPU Clock Frequency

The FRAM controller uses a 2-way associative cache that has a 64-bit line size. The cache uses static RAM to store pre-fetched instructions. Figure 3 shows a block diagram of the FRAM controller. The function of the FRAM controller is to pre-fetch four instruction words depending on the current PC location. The actual execution of these instructions is carried out in the cache. Once the end of the cache buffer is reached, the FRAM controller preserves the four current words in one page of the cache and fetches the next four words. If a code discontinuity is encountered at the end of a two-page cache, the cache is refreshed and the following four words of instruction are retrieved from FRAM. However, if the application code loops back to a location already present in the cache at the end of the cache, the relevant instruction is simply executed directly from the cache instead of re-fetching code from FRAM.

Note that only FRAM accesses are subject to the 8 MHz access limitation. A system clock of up to 24 MHz can be used when executing from the cache, which significantly increases the throughput of code execution. Wait states are inserted only when the FRAM needs to be accessed to refresh the cache, i.e., when a code discontinuity is encountered. Also, the FRAM controller makes use of the cache efficiently in the background in a way that is transparent to the user.

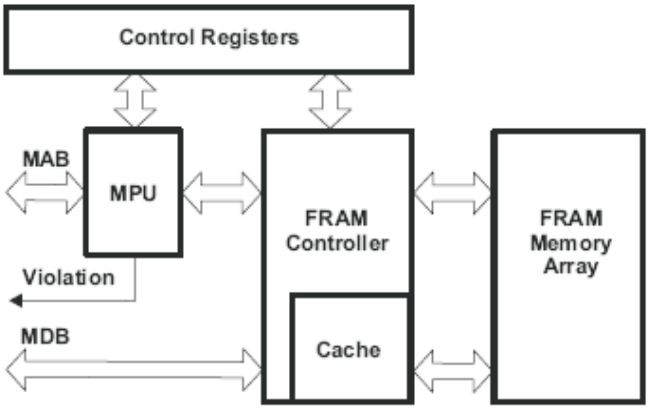

Figure 3. FRAM Controller Block Diagram

However, it is good practice to write short, efficient loops to achieve the maximum benefit of executing code from the cache and to minimize cache refreshes. Note that the cache is for instructions only and any data will be fetched directly from the FRAM. Executing from the cache makes the system more optimized for speed and power because:

- Power is significantly lower when executing code from cache
- The execution throughput is not limited to 8 MHz, thereby, maximizing the FRAM write speed

When writing to FRAM, bench tests were performed using different MCLK frequencies of 8 MHz, 16 MHz and 24 MHz using DMA with varying block sizes. The results are shown in Figure 4.

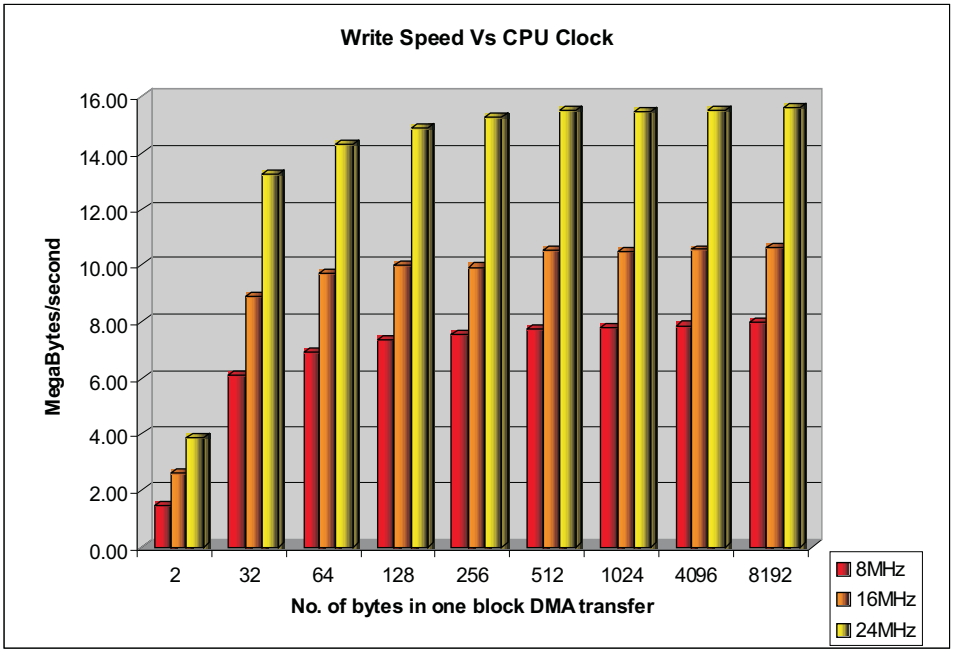

Figure 4. FRAM Write Speed vs. CPU Clock Frequency (MCLK)

In the chart, data for f_{MCLK} = 8 MHz is the same as in Figure 2. The orange and yellow bars illustrate the maximum FRAM write speed when f_{MCLK} = 16 MHz and 24 MHz, respectively.

Consider the data point for DMA block size = 512 bytes:

Speed at f_{MCLK} = 8 MHz: 7 MBps

Speed at f_{MCLK} = 16 MHz: 10 MBps

Speed at f_{MCLK} = 24 MHz : 15 MBps

This data shows that by increasing the MCLK frequency by a factor of 3, the FRAM write speed does not increase proportionally. That is because only the access to RAM and the instruction fetches in cache are executed at 24 MHz. Any access to FRAM is still performed at 8 MHz. Therefore, only a portion of the entire block write benefits from the f_{MCLK} increase. However, the throughput increase (not 1:1) is still significant, resulting in almost double the FRAM write speed at three times the MCLK frequency.

Consider a second data point where DMA transfer size is 8KB. At f_{MCLK} = 24 MHz, the FRAM write speed is very close to the theoretical maximum of 16 MBps. However, before it is assumed this as the de facto standard, a few words of caution:

- The speed of FRAM access at f_{MCLK} > 8 MHz and the length of wait states is dependent on factors such as V_{CC} , temperature, and process variation. The length of the wait states can be fixed by using manual wait state control option; however, there is still some possibility for variation in the overall FRAM write speed. While 16 MBps is achievable, it is not guaranteed and there may be a per device variation.
- The data presented above is an average from bench testing a limited number of device samples. The intent was to test the boundaries of FRAM write speed and not to provide a specification for the maximum write speed. The maximum write speed is highly application dependent, based on data and code overhead, block sizes and other system parameters.

3 Conclusion

FRAM is undoubtedly the fastest non-volatile embedded memory option available today. Being embedded with the ultra-low power MSP430 architecture makes it a perfect choice for applications needing extremely fast write speeds, low power and high endurance. Some of these applications include data logging using remote sensors, energy harvesting applications, and critical response time applications. The key factors that influence the maximum possible FRAM write throughput were discussed and the tradeoffs presented. In analyzing the bench test results for the MSP430FR5739, it is seen that the achievable practical write speed is very close to the theoretical maximum. It is up to the user to determine the available resources and architect their application in a way that can achieve the fastest possible write speed for FRAM.

4 References

1. *MSP430FR5xx Family User's Guide* (SLAU272)
2. *MSP430FR573x, MSP430FR572x Mixed Signal Microcontroller Data Sheet* (SLAS639)
3. *MSP430F543xA, MSP430F541xA Mixed Signal Microcontroller Data Sheet* (SLAS655)
4. *Migrating From the MSP430F2xx Family to the MSP430FR57xx Family* (SLAA499)
5. *MSP430F22x2, MSP430F22x4 Mixed Signal Microcontroller Data Sheet* (SLAS504)

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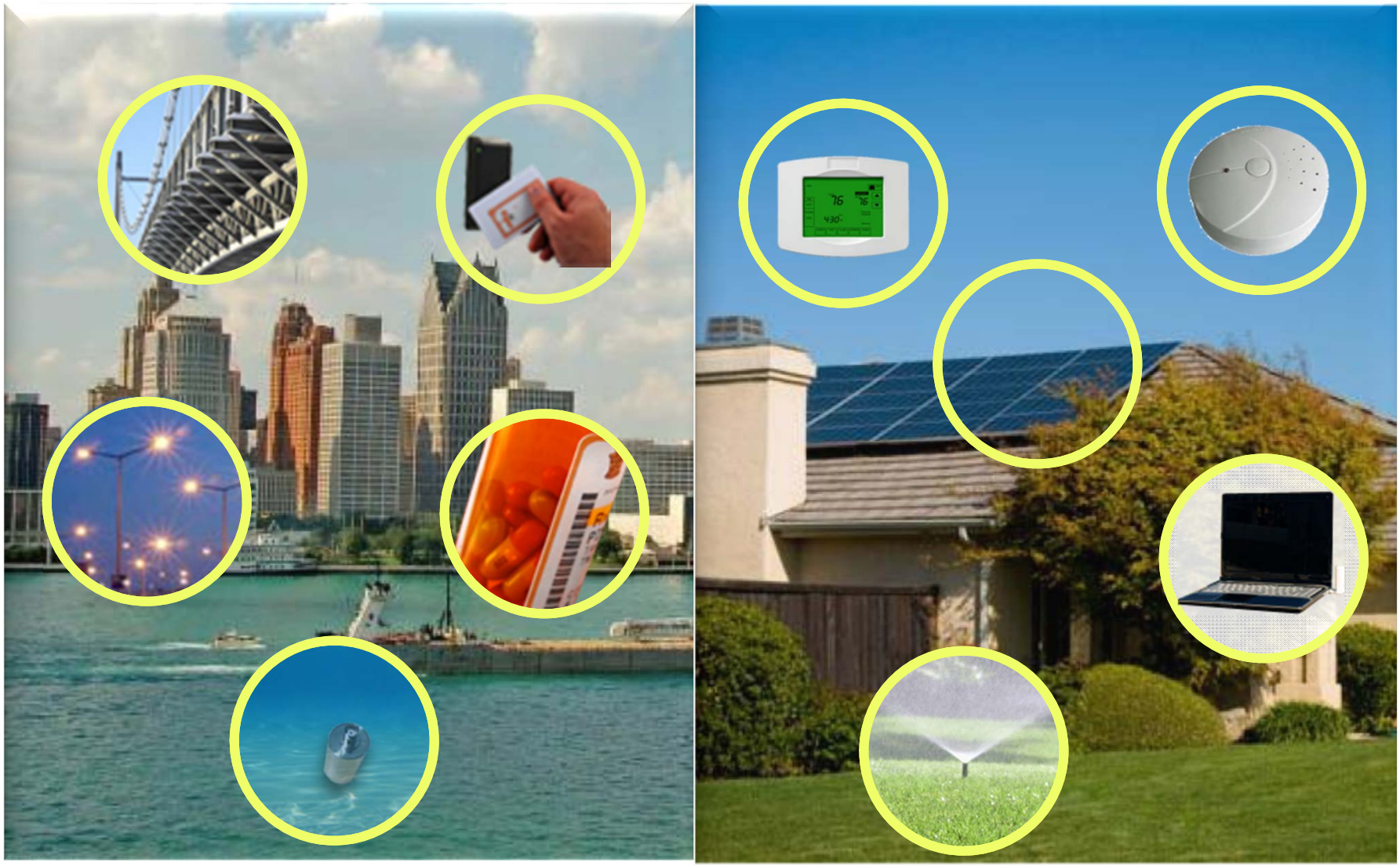
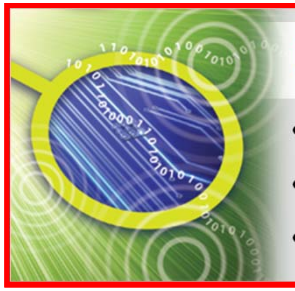
Make the world smarter with industry's first ultra-low-power FRAM microcontroller from TI

Make it smarter: More sensors. More data.



Industry's first ultra-low-power FRAM MCU

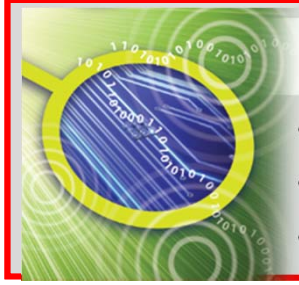


More sensors in new places with ultra-low-power memory

- Write up to 100x times faster and save as much as 250x power
- Virtually unlimited write endurance
- Non-volatile memory: data retention possible in ALL power modes

Experience unparalleled freedom with unified memory

- Easily change memory partitioning in software
- Eliminate need for separate EEPROM and battery-backed SRAM

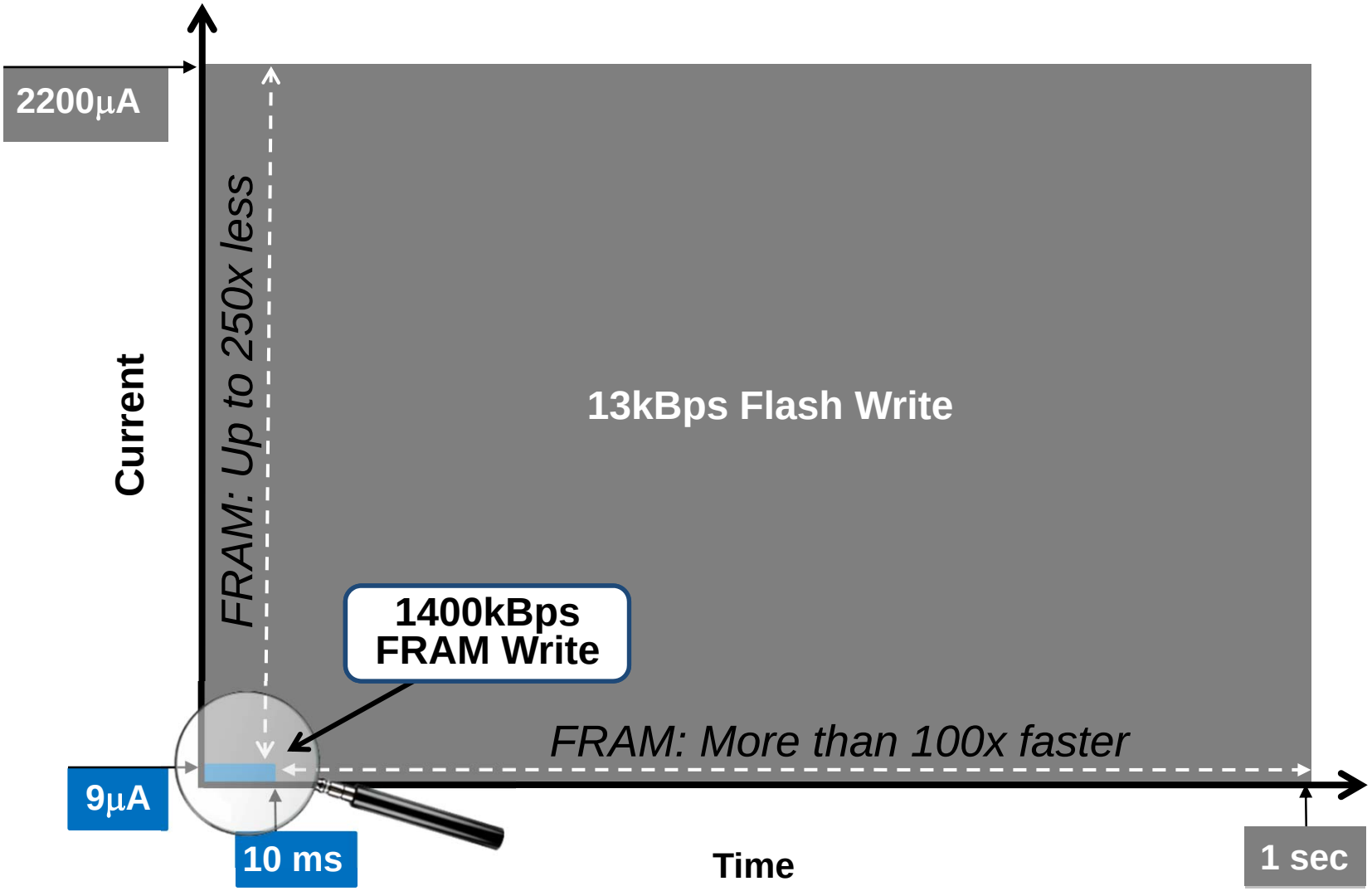


Speed up designs – Tools, software and system solution

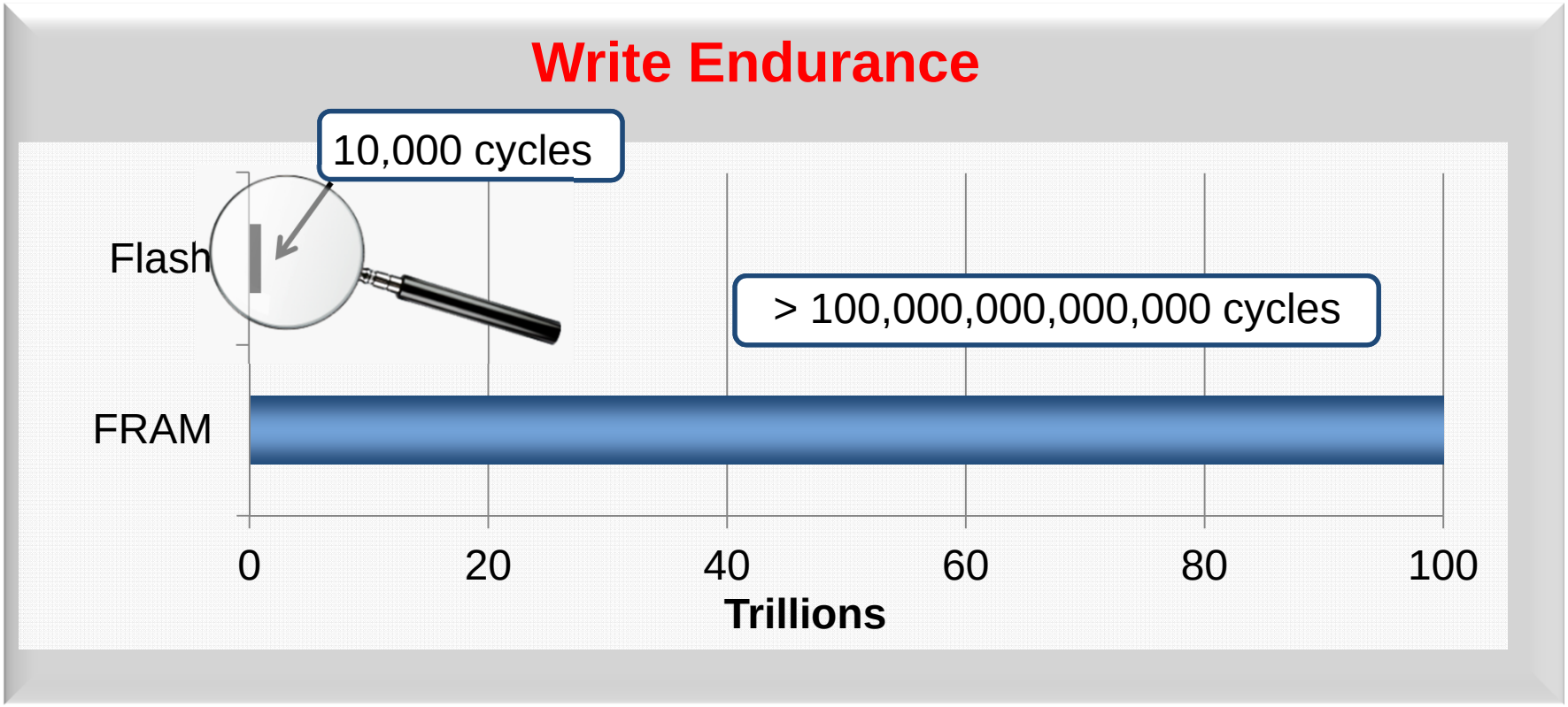
- Low cost development kits and code compatibility across MSP platform
- Industry's broadest RF technology & tools portfolio
- Training and documentation

Texas Instruments

MSP430FR57xx in the energy plane enables more sensors in new places



Continuous ultra-low-power data logging



Supports more than 150,000 years of continuous data logging
(vs. less than 7 minutes with Flash)

All-in-one: FRAM MCU delivers max benefits

	FRAM	SRAM	EEPROM	Flash
Non-volatile Retains data without power	Yes	No	Yes	Yes
Write speeds (13KB)	10ms	<10ms	2secs[1]	1 sec
Average active Power [µA/MHz]	110	<60	50mA+[1,2]	260
Write endurance	100 Trillion+	Unlimited	100,000	10,000
Dynamic Bit-wise programmable	Yes	Yes	No	No
Unified memory Flexible code and data partitioning	Yes	No	No	No

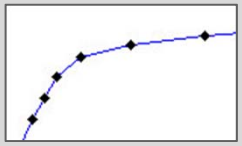
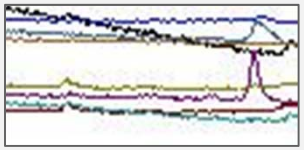
1 – Standalone EEPROM Write

2 – Total power consumption

Data for FRAM, SRAM and Flash are representative of embedded memory performance within device

FRAM solves real-world challenges

Sensor Datalogging

Challenge	FRAM solution
Power consumption limits locations, increases maintenance	Energy harvesting enables more sensors in more locations
Limited data update/ write speed	Continuous and reliable monitoring , storage and RF transmission
 Selective monitoring	 Continuous monitoring

Asset Tracking

Flow meters

Sports & Fitness

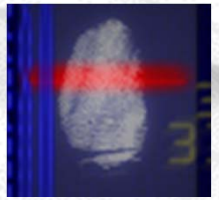
Seismic monitoring

Over-the-air updates

Challenge	FRAM solution
Consume up to 1 month battery life	Uses less than ¼ day of battery life
Block level erase & program	Bit level access
Need redundant (mirror) memory blocks	Write guarantee in case of power loss

Home automation

Metering



Safety & security

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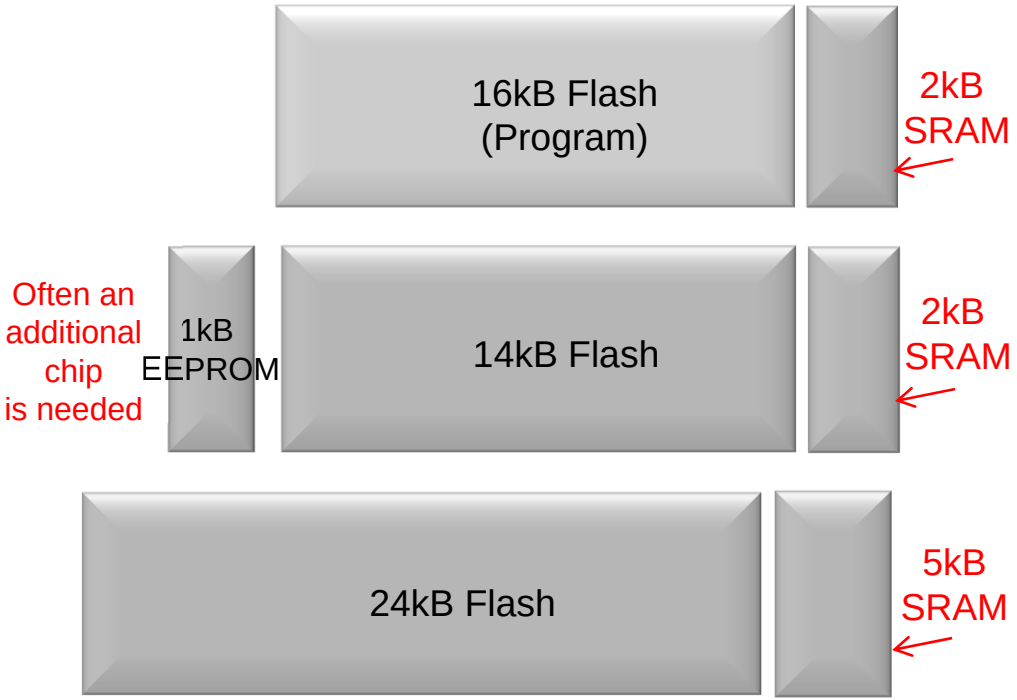
Unified memory: Another dimension of freedom for software developers

Before FRAM

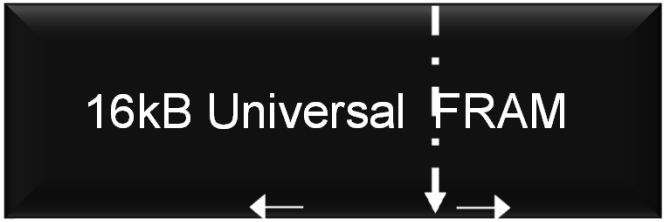
Multiple device variants may be required



To get more SRAM you may have to buy 5x the needed FLASH ROM

With FRAM

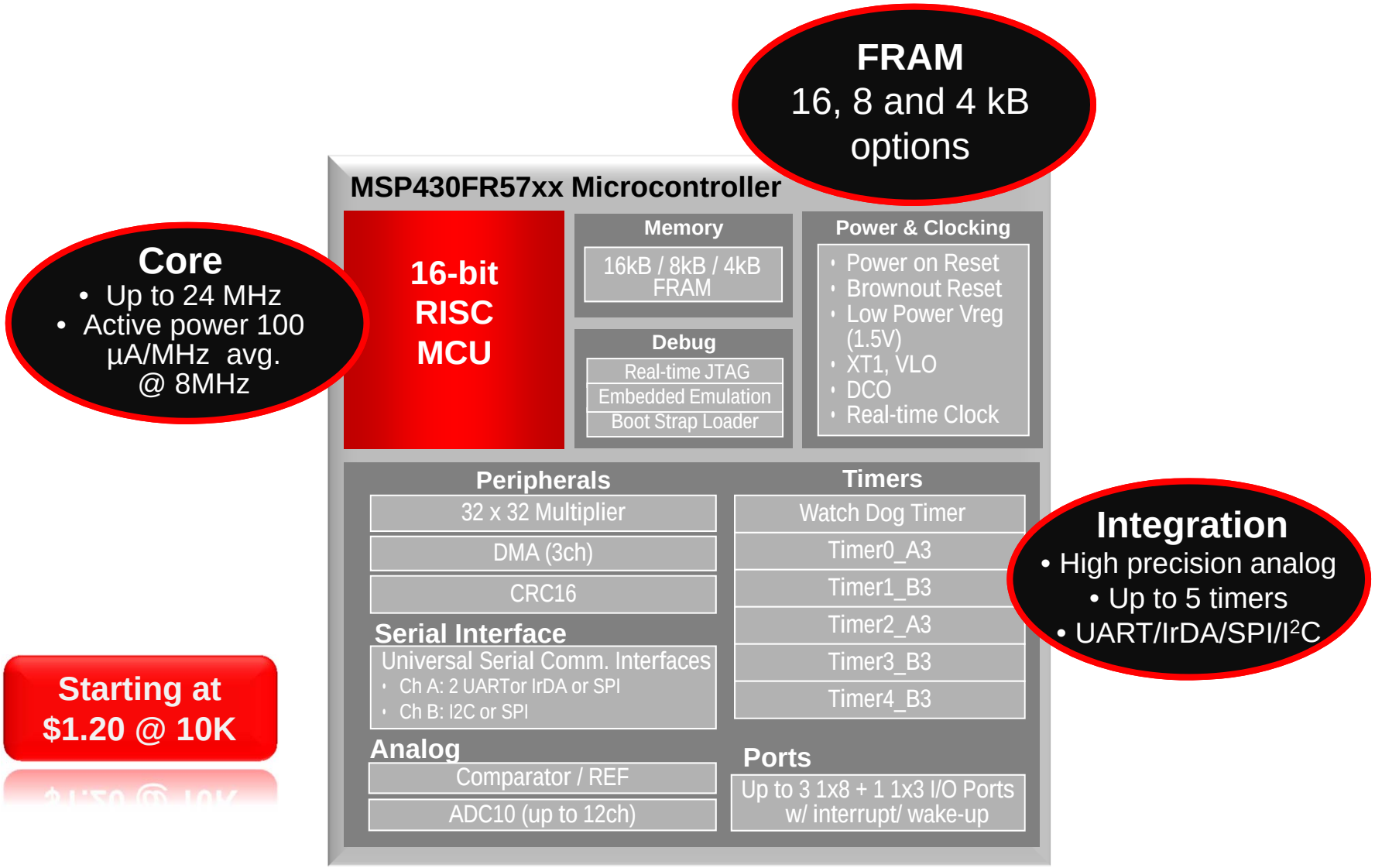
One device supporting multiple options “slide the bar as needed”



Data vs. program memory partitioned as needed

- Easier, simpler inventory management
- Lower cost of issuance / ownership
- Faster time to market for memory modifications

Industry's first ultra-low-power FRAM MCU



Speed design with tools, software and system solution

Get started in less than 10 minutes

MSP-EXP430FR5739 Experimenter's Kit

- Preloaded "User Experience" Demo code
- On board emulation, LPM measurement,
- Accelerometer, 8 LEDs, switch buttons
- Connect to other MSP430 boards and TI wireless portfolio

Price: $29.00

MSP-TS430RHA40A Development Kit

- 40-pin ZIF socket target board used to program and debug the MSP430 in-system through the JTAG interface

Price: $99

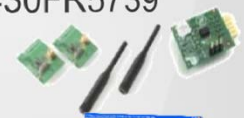
System solution

- TI offers the Industry's broadest RF portfolio

ZigBee™ · 6LoWPAN · <1GHz · Wi Fi · Bluetooth Low Energy · ANT+ · RF4CE · PurePath Wireless Audio · Bluetooth · GPS

- With hardware modules compatible with the MSP-EXP430FR5739





- With RF design tools

- With reference designs, software & complete ecosystem

Making RF connectivity easy & affordable

- Code libraries
- IAR-EW430 v5.20.x supporting FRAM devices
- CCS v4.2.3 supporting FRAM devices
- Comprehensive application and "How to" notes

More info at:
www.ti.com/fram

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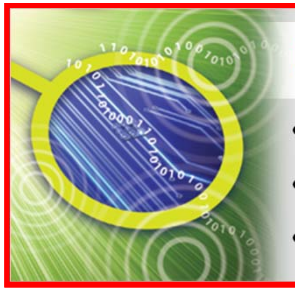
Industry's first ultra-low-power FRAM MCU



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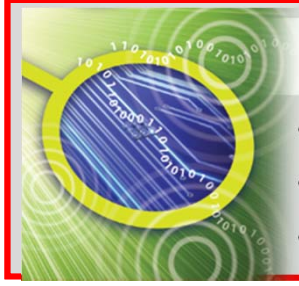

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- Industry's broadest RF technology & tools portfolio
- Training and documentation

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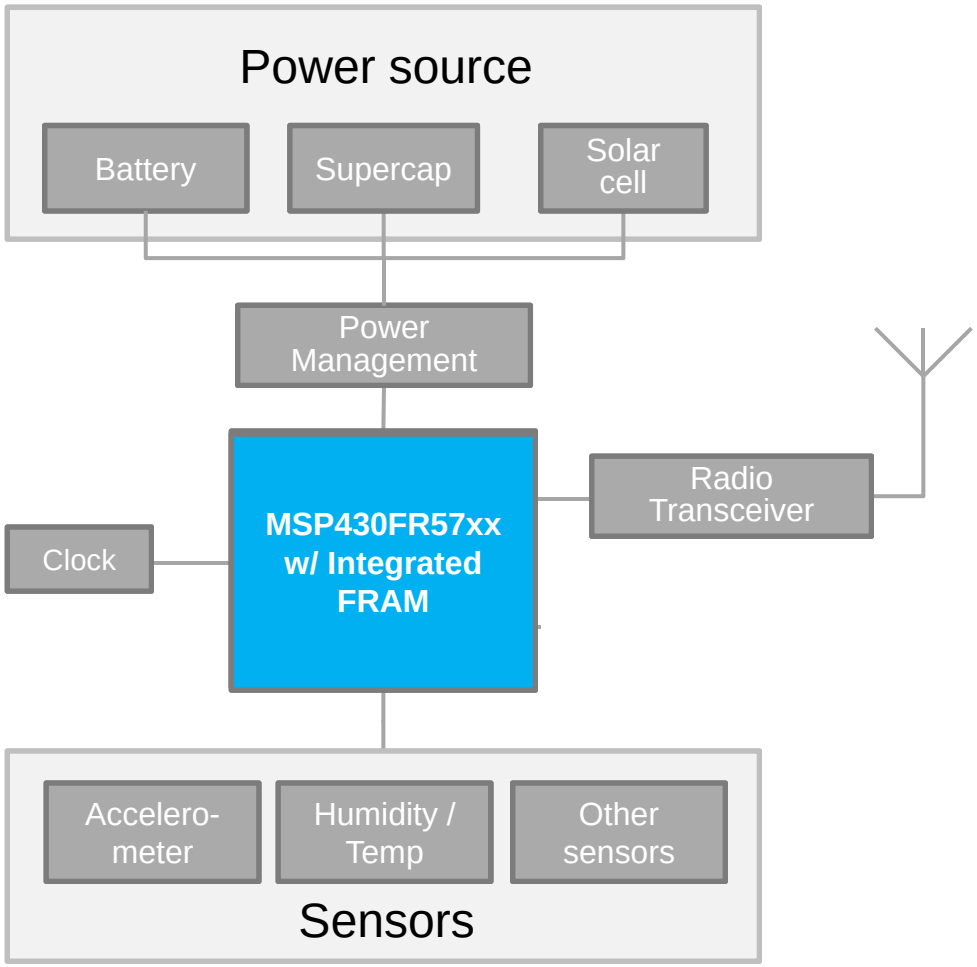
Backup

Seismic Monitoring Systems



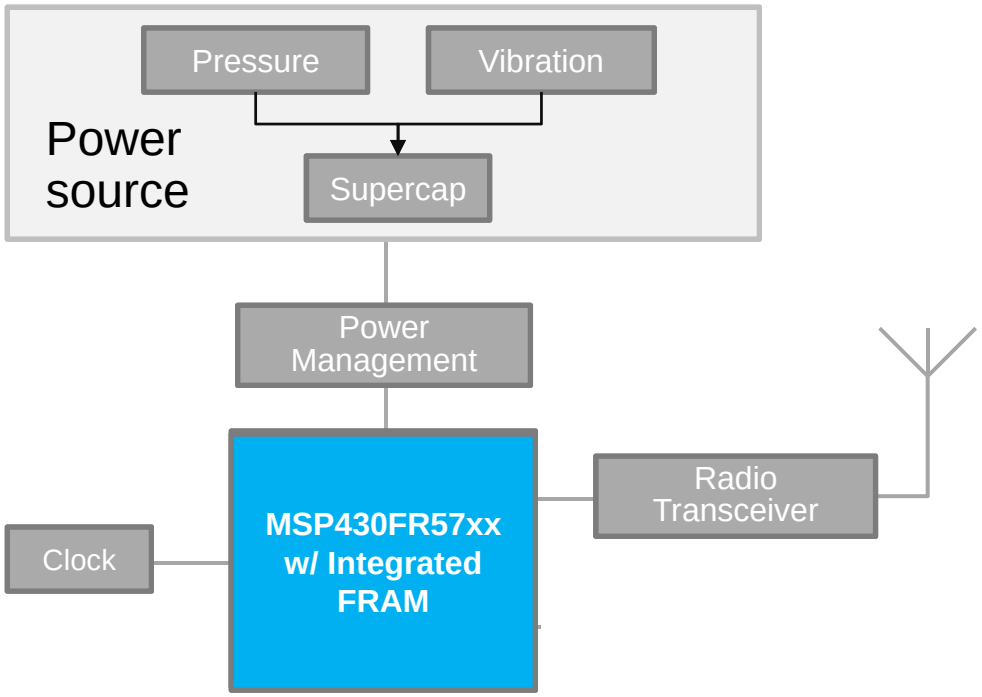
Needs

- Accurate, fast, robust data recording on board from multiple sensors
- Ultra low power operation
  - Maximize battery life
  - Enable advanced processing on board
- Maximize data storage capability
  - Increased sensor life
  - Reduce maintenance

MSP430FR57xx delivers

- Instant, robust writes – even on power loss
- Ultra low power writes – 100x< Flash/EEPROM
  - Save power to enable advanced processing on board within same power budget
  - Increase battery life
- Virtually unlimited writes
  - Reduce BOM (external EEPROM)
  - Reduce sensor replacement

Batteryless Intelligent Energy Harvesting Switch



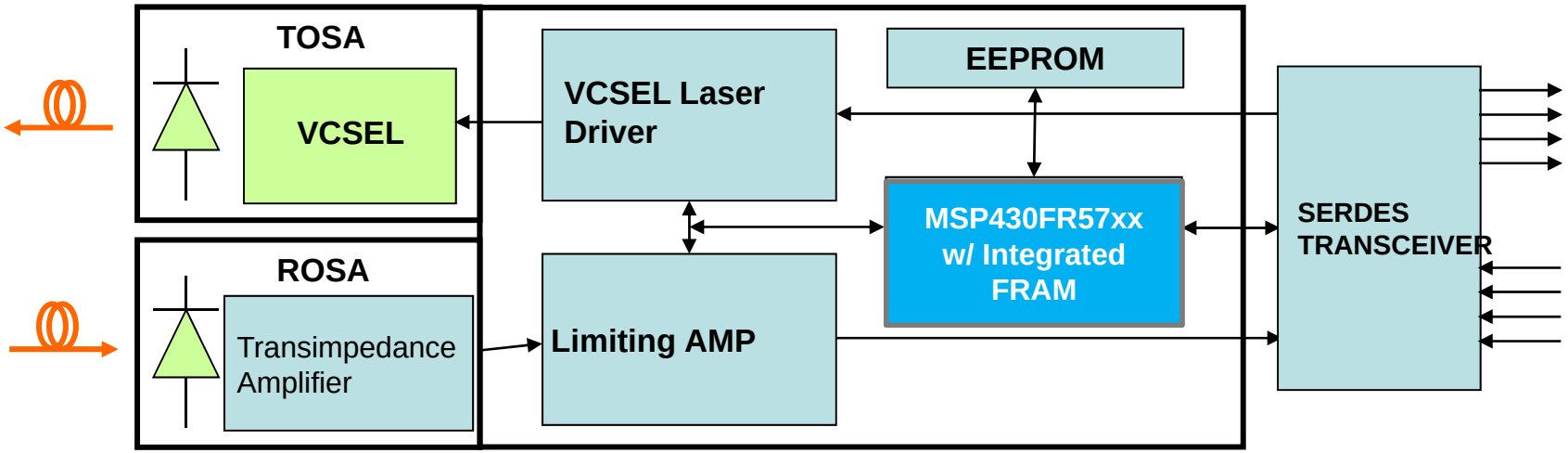
Needs

- Accurate, fast, robust data recording on status
  - Intelligent status processing and transmission
- Ultra low power operation
  - Enable advanced processing on board → minimum power consumption for MCU
- Maximize data storage capability
  - Increased device life
  - Reduced maintenance

MSP430FR57xx delivers

- Instant, robust writes – even on power loss
- Ultra low power writes – 100x< Flash/EEPROM
  - Save power to enable advanced processing & RF transmission on board within same power budget
- Virtually unlimited writes
  - Reduce sensor replacement – lower maintenance cost

SFP+ Optical Network Switch Modules



Needs

- Accurate, fast, robust data access
- Cost sensitive
- Small Footprint

MSP430FR57xx delivers

- Granular, fast memory access
  - >100 trillion read/write cycles
- Remove external EEPROM & lower test costs
- Reduced material count

Videos

Please visit

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